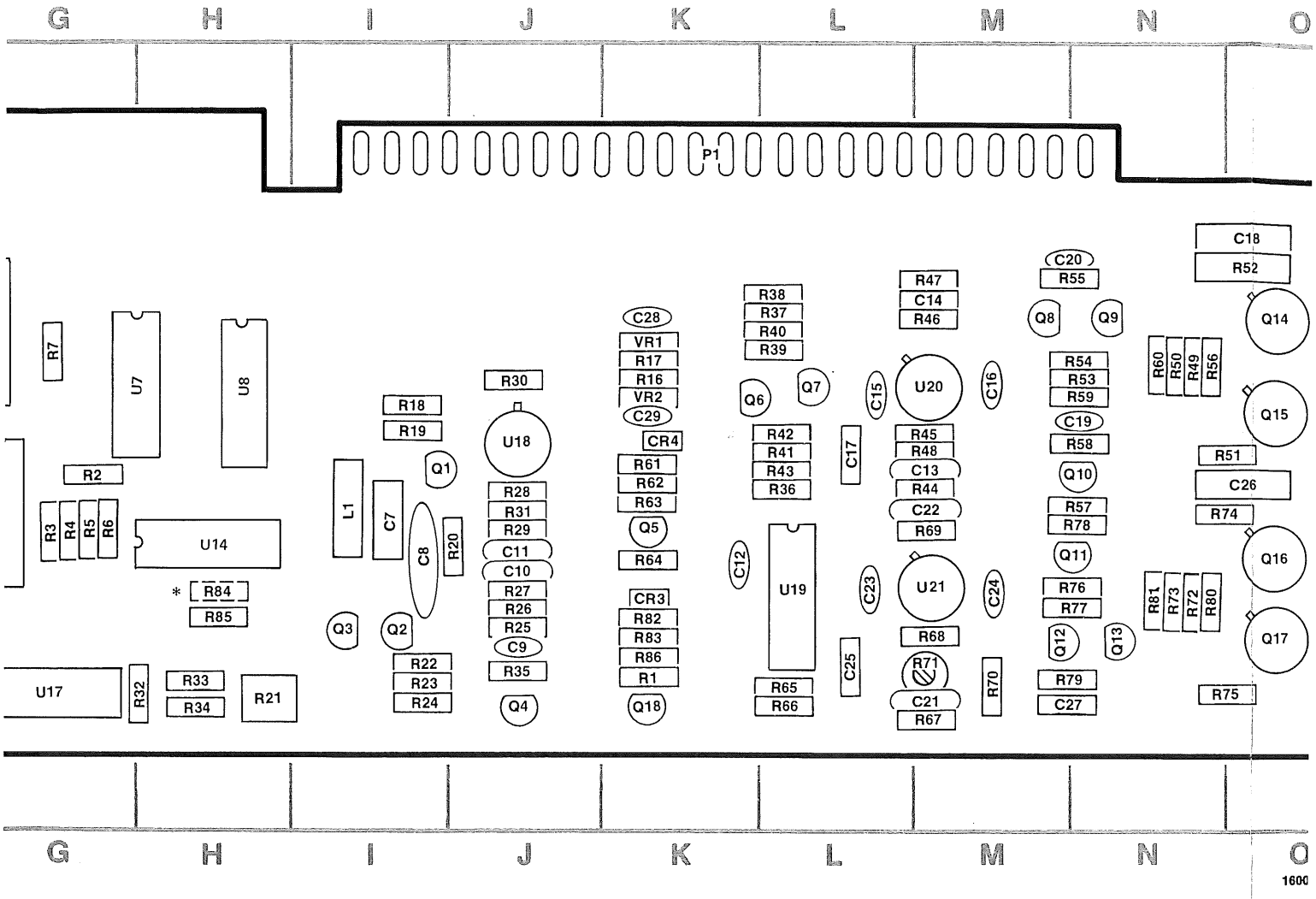
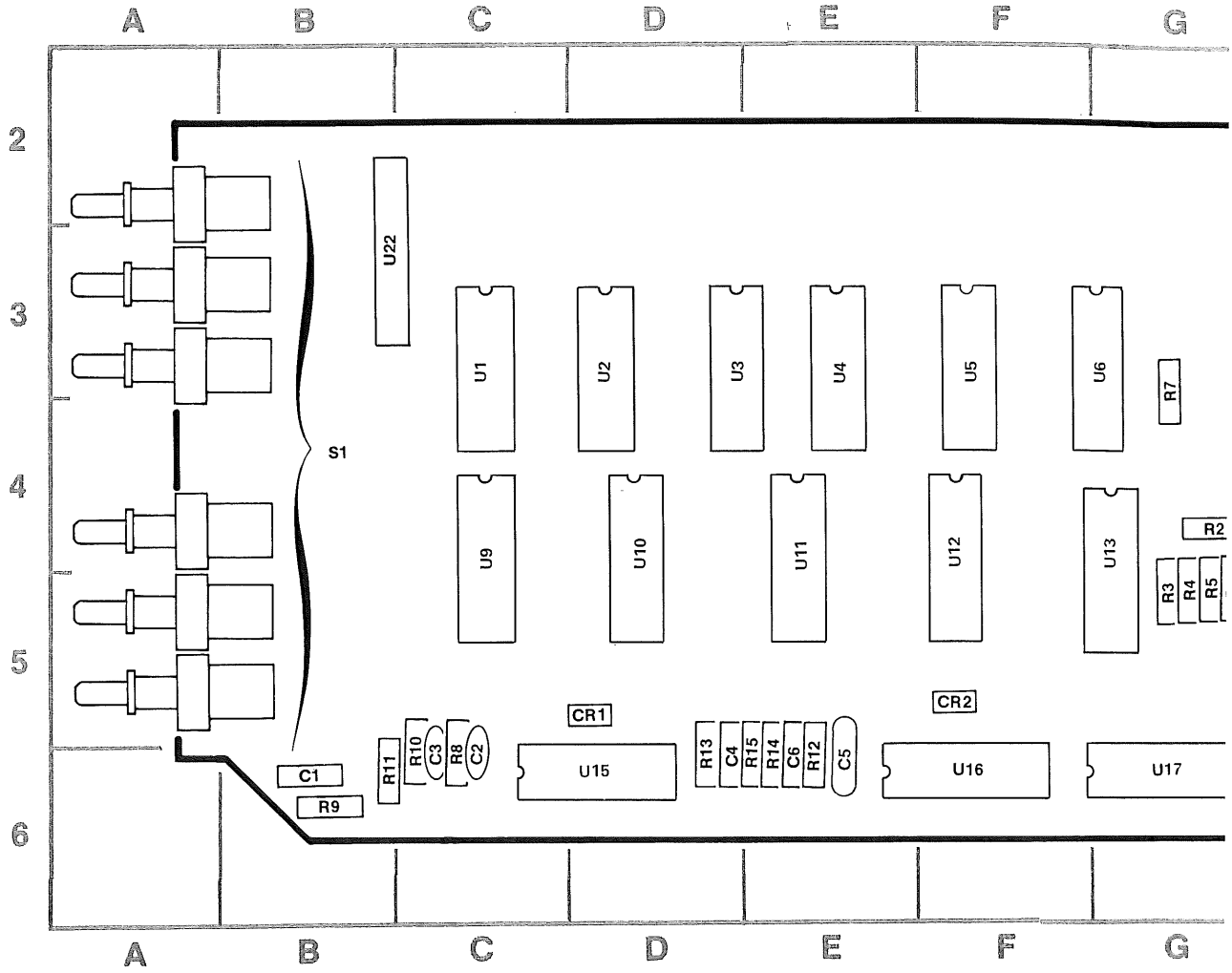


GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
N-5	R11	C-6	R27	J-5	R44	M-4	R61	K-4	R78	N-5	U8	H-4
O-3	R12	E-6	R28	J-4	R45	M-4	R62	K-4	R79	N-6	U9	C-4
O-4	R13	D-6	R29	J-5	R46	M-3	R63	K-4	R80	N-5	U10	D-4
O-5	R14	E-6	R30	J-4	R47	M-3	R64	K-5	R81	N-5	U11	E-4
O-5	R15	E-6	R31	J-5	R48	M-4	R65	L-6	R82	K-5	U12	F-4
K-6	R16	K-4	R32	H-6	R49	N-4	R66	L-6	R83	K-5	U13	G-4
K-6	R17	K-4	R33	H-6	R50	N-4	R67	M-6	R84*	H-5	U14	H-5
G-4	R18	I-4	R34	H-6	R51	N-4	R68	M-5	R85	H-5	U15	D-6
G-5	R19	I-4	R35	J-6	R52	O-3	R69	M-5	R86	K-5	U16	F-6
G-5	R20	J-5	R36	L-4	R53	N-4	R70	M-6	S1	B-4	U17	G-6
G-5	R21	H-6	R37	L-3	R54	N-4	R71	M-5	U1	C-3	U18	J-4
G-5	R22	I-5	R38	L-3	R55	M-3	R72	N-5	U2	D-3	U19	L-5
G-3	R23	I-6	R39	L-3	R56	N-4	R73	N-5	U3	D-3	U20	M-4
C-6	R24	I-6	R40	L-3	R57	N-4	R74	N-4	U4	E-3	U21	M-5
B-6	R25	J-5	R41	L-4	R58	N-4	R75	N-6	U5	F-3	U22	C-3
C-6	R26	J-5	R42	L-4	R59	N-4	R76	N-5	U6	G-3	VR1	K-3
			R43	L-4	R60	N-4	R77	N-5	U7	H-4	VR2	K-4



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	D
C1	B-6	C17	L-4	CR4	K-4	Q13	N-5	F
C2	C-6	C18	O-3	L1	I-4	Q14	O-3	F
C3	C-6	C19	N-4	P1	K-2	Q15	O-4	F
C4	D-6	C20	M-3	P2	O-4	Q16	O-5	F
C5	E-6	C21	M-6	Q1	I-4	Q17	O-5	F
C6	E-6	C22	M-4	Q2	I-5	Q18	K-6	F
C7	I-5	C23	L-5	Q3	I-5	R1	K-6	F
C8	I-5	C24	M-5	Q4	J-6	R2	G-4	F
C9	J-5	C25	L-5	Q5	K-5	R3	G-5	F
C10	J-5	C26	O-4	Q6	K-4	R4	G-5	F
C11	J-5	C27	N-6	Q7	L-4	R5	G-5	F
C12	K-5	C28	K-3	Q8	M-3	R6	G-5	F
C13	M-4	C29	K-4	Q9	N-3	R7	G-3	F
C14	M-3	CR1	D-5	Q10	N-4	R8	C-6	F
C15	L-4	CR2	F-5	Q11	N-5	R9	B-6	F
C16	M-4	CR3	K-5	Q12	N-5	R10	C-6	F

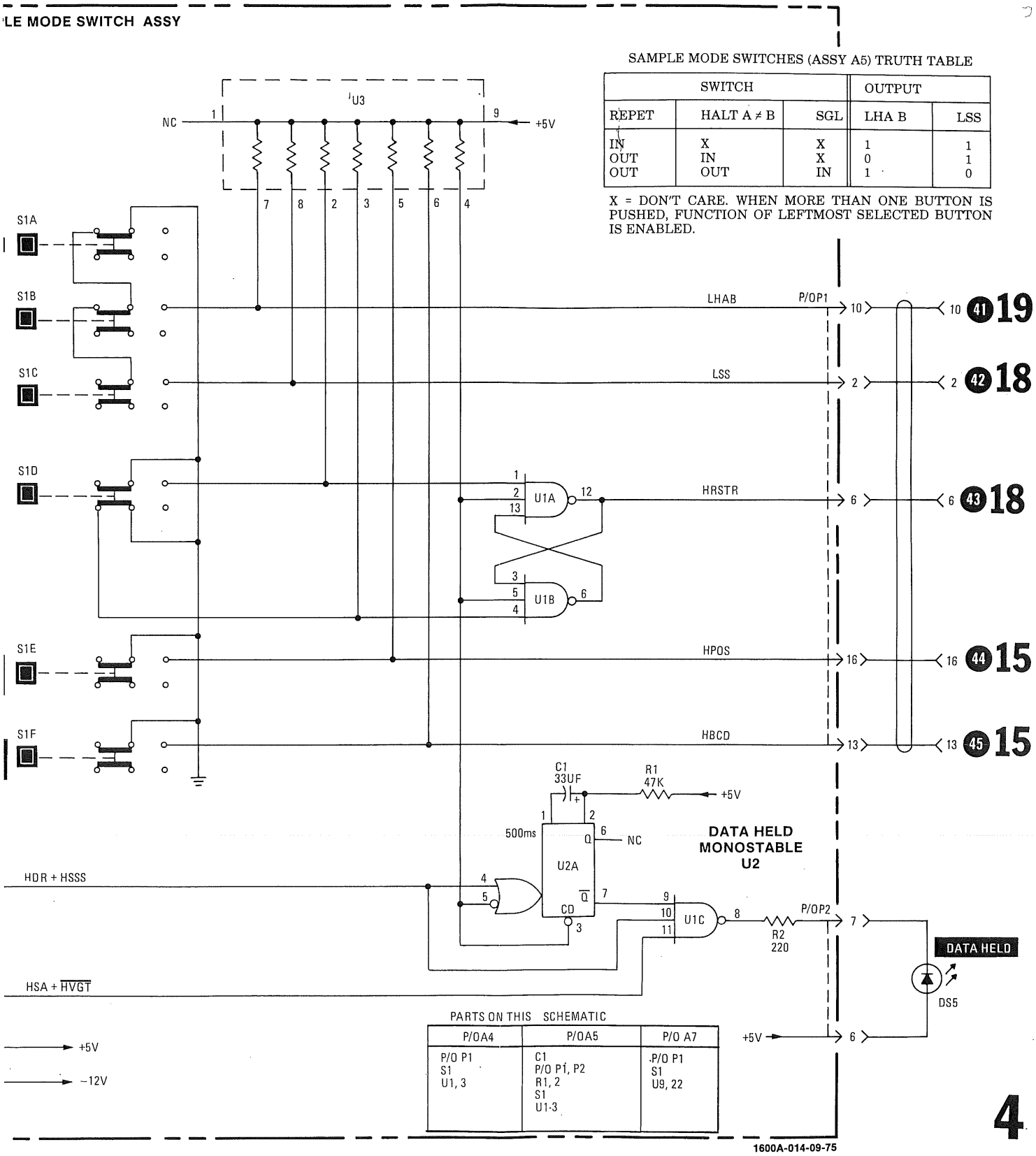
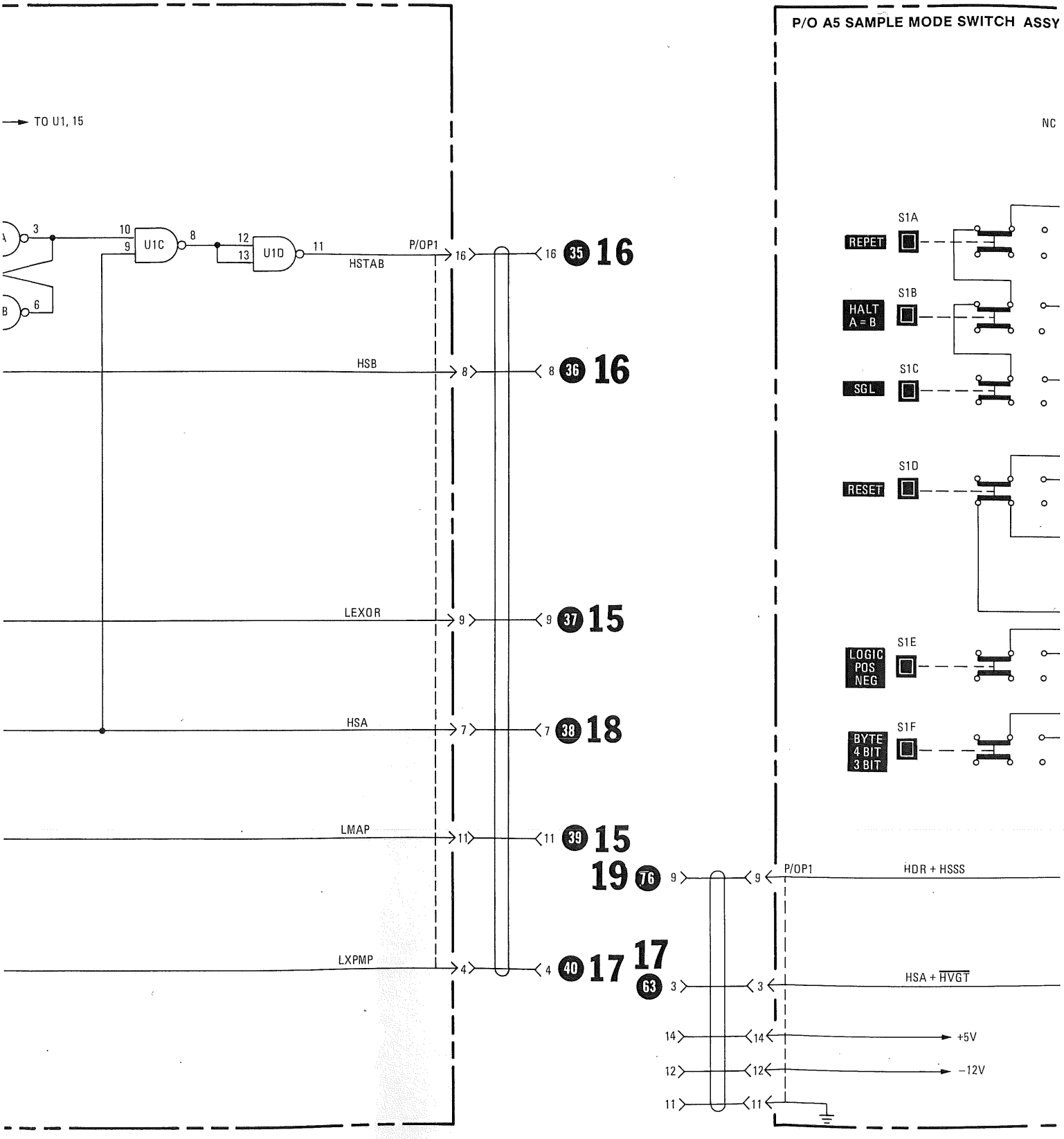


Figure 8-14.
Schematic 4, Display and Sample Mode Switches


P/O A5 SAMPLE MODE SWITCH ASSY
TO U1, 15
NC
U1C
U1D
HSTAB
P/OP1
HSB
LEXOR
HSA
LMAP
LXPMP
S1A
REPET
S1B
HALT A=B
S1C
SGL
S1D
RESET
S1E
LOGIC POS NEG
S1F
BYTE 4 BIT 3 BIT
HDR + HSSS
HSA + HVGT
+5V
−12V

15

86 8

87 8

88 8

89 8

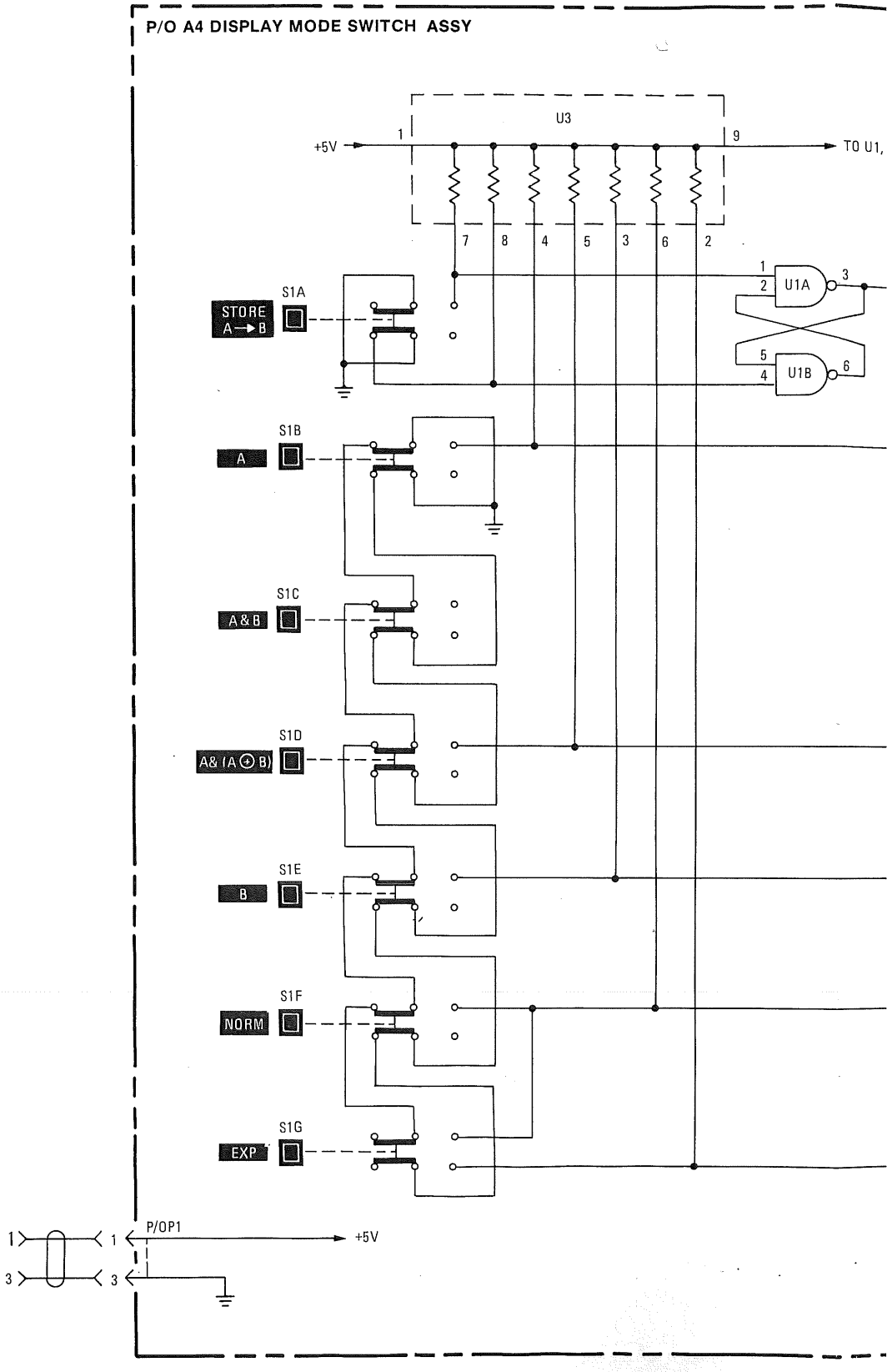
90 17

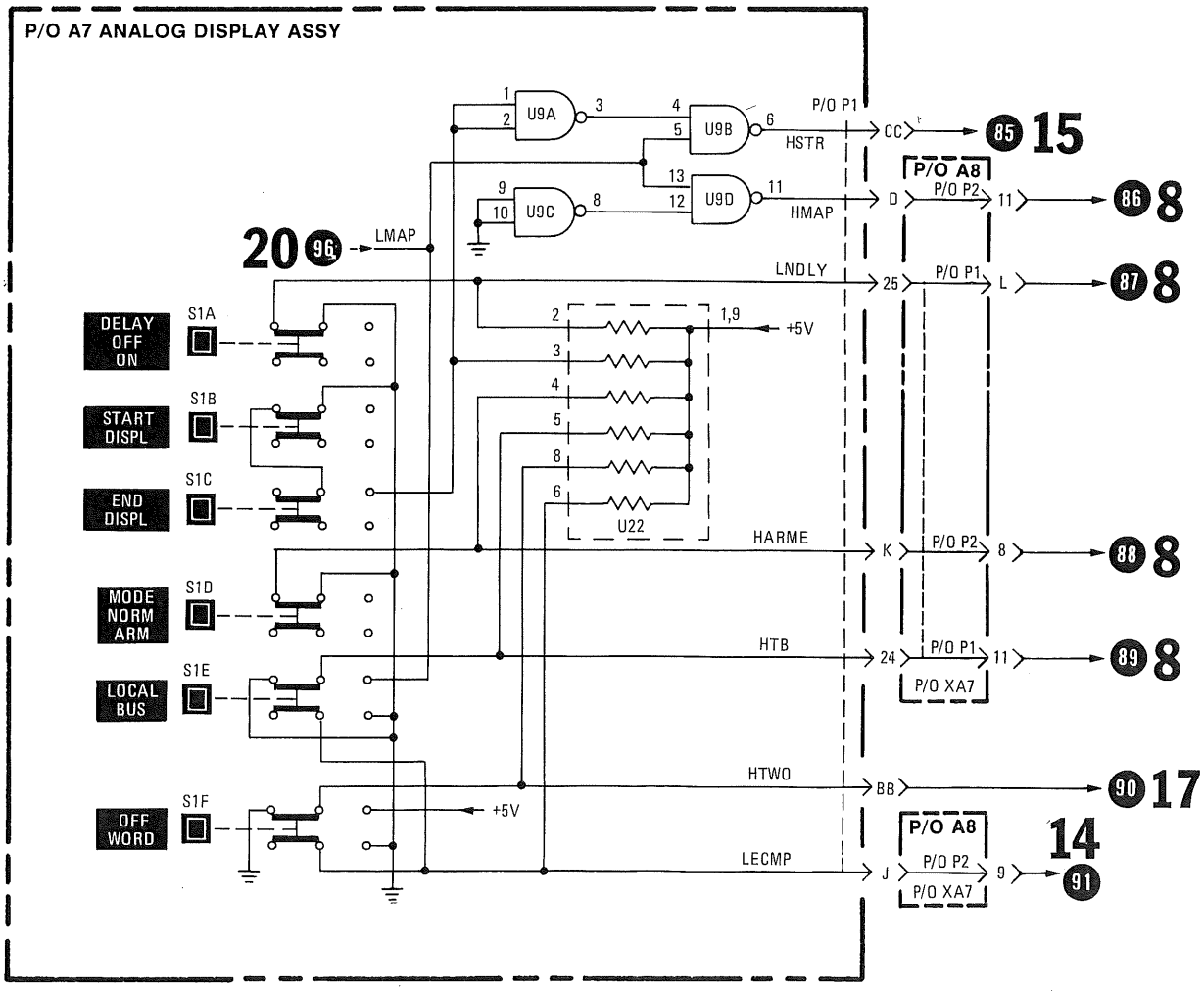
14

91

MAP	LXPMP
	1
	1
	1
	1
	1
	0

OF LEFTMOST SE-





DISPLAY MODE SWITCH ASSY A4 TRUTH TABLE

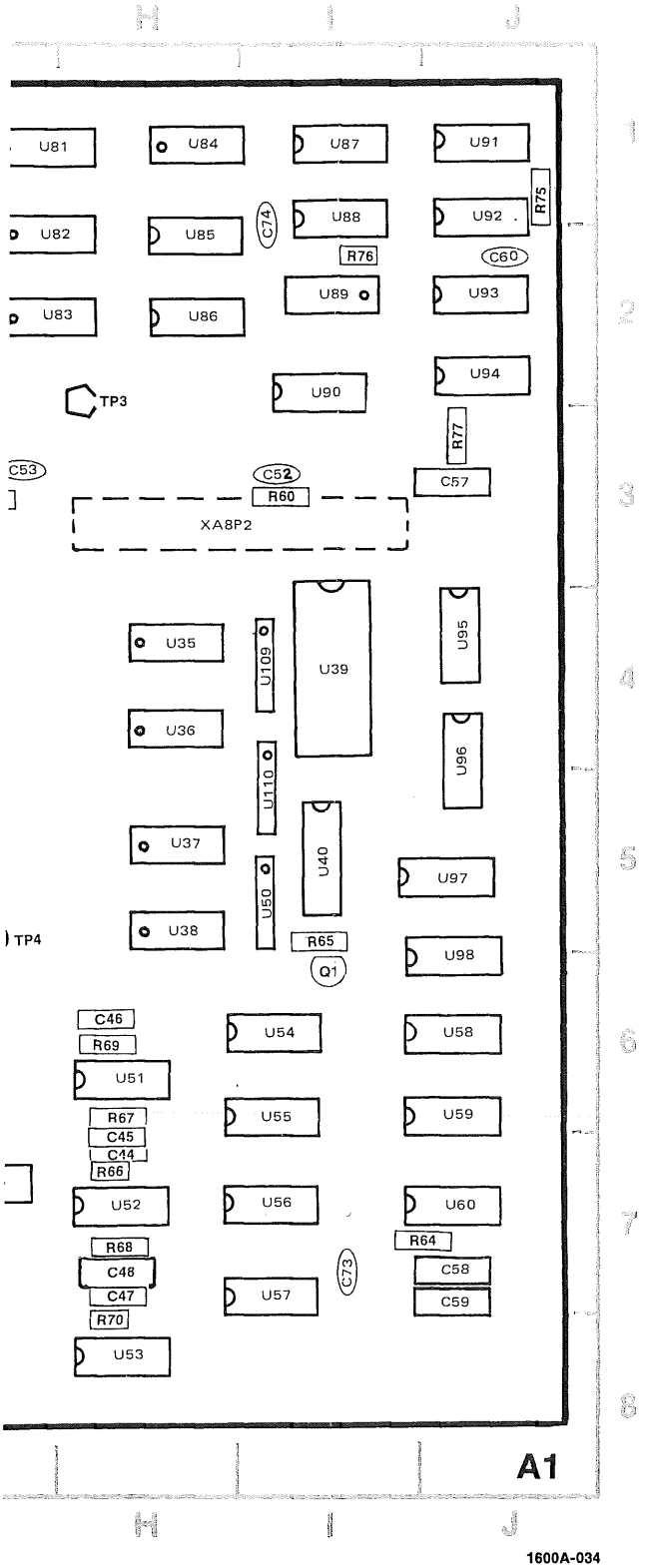
SWITCH						OUTPUT				
A	A & B	A & (A⊕B)	B	NORM	EXP	HSB	LEXOR	HSA	LMAP	LXPMP
IN	X	X	X	X	X	0	1	1	1	1
OUT	IN	X	X	X	X	1	1	1	1	1
OUT	OUT	IN	X	X	X	1	0	1	1	1
OUT	OUT	OUT	IN	X	X	1	1	0	1	1
OUT	OUT	OUT	OUT	IN	X	1	1	1	0	1
OUT	OUT	OUT	OUT	OUT	IN	1	1	1	0	0

X = DON'T CARE. WHEN MORE THAN ONE BUTTON IS PUSHED, FUNCTION OF LEFTMOST SELECTED BUTTON IS ENABLED.

NOTE
See Fig. 8-15 For A1 Parts Identification

EF SIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
4	J-7	U25	C-3	U69	D-1
5	I-5	U26	D-7	U70	D-2
6	H-7	U27	D-7	U71	D-3
7	H-6	U28	G-4	U72	E-1
8	H-7	U29	G-4	U73	E-1
9	H-6	U30	G-5	U74	E-2
0	H-8	U31	G-5	U75	E-2
1	G-3	U32	G-6	U76	E-3
2	C-7	U33	G-6	U77	F-1
3	C-7	U34	G-6	U78	F-1
4	C-8	U35	H-4	U79	F-2
5	J-1	U36	H-4	U80	F-3
6	I-2	U37	H-5	U81	G-1
7	J-3	U38	H-5	U82	G-2
8	B-1	U39	I-4	U83	G-2
	A-8	U40	I-5	U84	H-1
1	C-8	U41	C-7	U85	H-2
2	C-7	U42	C-8	U86	H-2
3	H-2	U43	D-8	U87	I-1
4	G-5	U44	E-8	U88	I-1
	C-3	U45	F-8	U89	I-2
	C-4	U46	G-8	U90	I-2
	C-4	U47	F-7	U91	J-1
	C-4	U48	G-7	U92	J-1
	C-5	U49	G-7	U93	J-2
	C-5	U50	I-5	U94	J-2
	C-6	U51	H-6	U95	J-4
	C-6	U52	H-7	U96	J-4
	C-6	U53	H-8	U97	J-5
0	D-3	U54	I-6	U98	J-6
1	D-4	U55	I-6	U99	E-4
2	D-4	U56	I-7	U100	E-5
3	D-4	U57	I-7	U101	E-6
4	D-5	U58	J-6	U102	F-4
5	D-5	U59	J-6	U103	F-5
6	D-6	U60	J-7	U104	F-6
7	D-6	U61	B-1	U105	F-1
8	D-7	U62	B-1	U106	F-3
9	E-3	U63	B-2	U107	G-1
0	E-4	U64	B-2	U108	G-3
1	E-5	U65	C-1	U109	I-4
2	E-5	U66	C-2	U110	I-5
3	E-6	U67	C-2	XA8P1	F-3
4	E-6	U68	D-1	XA8P2	H-3

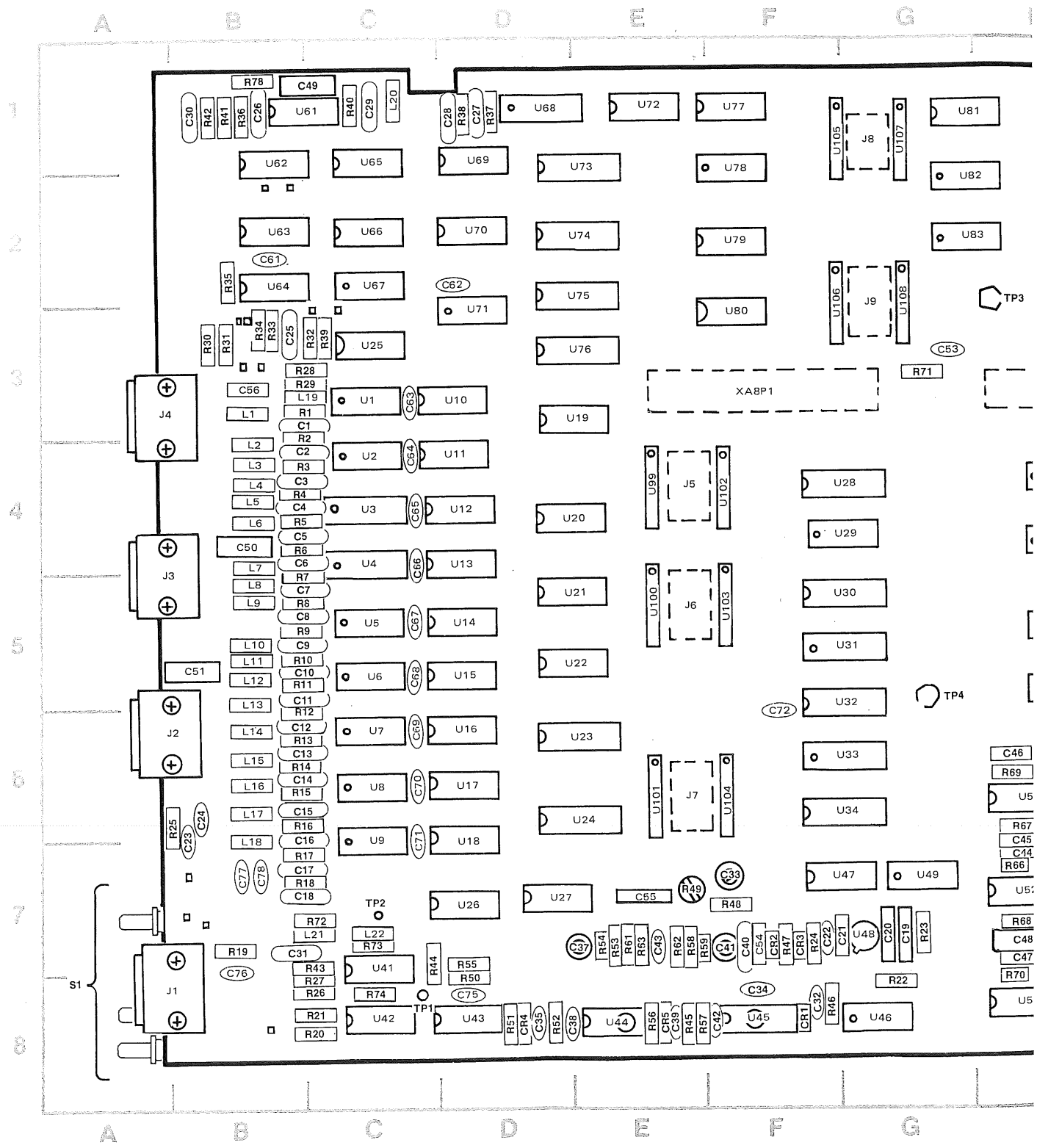
ard Assembly A1



1600A-034

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	R DE
C1	B-3	C47	H-7	J8	G-1	R20	C-8	R64	J-7	U2
C2	B-4	C48	H-7	J9	G-3	R21	C-8	R65	I-5	U2
C3	B-4	C49	B-1	L1	B-3	R22	G-8	R66	H-7	U2
C4	B-4	C50	B-4	L2	B-4	R23	G-7	R67	H-6	U2
C5	B-4	C51	B-5	L3	B-4	R24	F-7	R68	H-7	U2
C6	B-4	C52	I-3	L4	B-4	R25	A-6	R69	H-6	U3
C7	B-5	C53	G-3	L5	B-4	R26	C-8	R70	H-8	U3
C8	B-5	C54	F-7	L6	B-4	R27	C-8	R71	G-3	U3
C9	B-5	C55	E-7	L7	B-4	R28	B-3	R72	C-7	U3
C10	B-5	C56	B-3	L8	B-5	R29	B-3	R73	C-7	U3
C11	B-5	C57	J-3	L9	B-5	R30	B-3	R74	C-8	U3
C12	B-6	C58	J-7	L10	B-5	R31	B-3	R75	J-1	U3
C13	B-6	C59	J-7	L11	B-5	R32	C-3	R76	I-2	U3
C14	B-6	C60	J-2	L12	B-5	R33	B-3	R77	J-3	U3
C15	B-6	C61	B-2	L13	B-5	R34	B-3	R78	B-1	U3
C16	B-6	C62	D-2	L14	B-6	R35	B-2	S1	A-8	U4
C17	B-7	C63	C-3	L15	B-6	R36	B-1	TP1	C-8	U4
C18	B-7	C64	C-4	L16	B-6	R37	D-1	TP2	C-7	U4
C19	G-7	C65	C-4	L17	B-6	R38	D-1	TP3	H-2	U4
C20	G-7	C66	C-4	L18	B-6	R39	C-3	TP4	G-5	U4
C21	F-7	C67	C-5	L19	B-3	R40	C-1	U1	C-3	U4
C22	F-7	C68	C-5	L20	C-1	R41	B-1	U2	C-4	U4
C23	B-6	C69	C-6	L21	B-7	R42	B-1	U3	C-4	U4
C24	B-6	C70	C-6	L22	C-7	R43	C-7	U4	C-4	U4
C25	B-3	C71	C-6	Q1	I-6	R44	C-7	U5	C-5	U4
C26	B-1	C72	F-6	R1	B-3	R45	E-8	U6	C-5	U5
C27	D-1	C73	I-7	R2	B-4	R46	F-8	U7	C-6	U5
C28	D-1	C74	I-1	R3	B-4	R47	F-7	U8	C-6	U5
C29	C-1	C75	D-8	R4	B-4	R48	F-7	U9	C-6	U5
C30	B-1	C76	B-7	R5	B-4	R49	E-7	U10	D-3	U5
C31	B-7	C77	B-7	R6	B-4	R50	D-8	U11	D-4	U5
C32	F-8	C78	B-7	R7	B-5	R51	D-8	U12	D-4	U5
C33	F-7	CR1	F-8	R8	B-5	R52	D-8	U13	D-4	U5
C34	F-8	CR2	F-7	R9	B-5	R53	E-7	U14	D-5	U5
C35	D-8	CR3	F-7	R10	B-5	R54	E-7	U15	D-5	U5
C37	E-7	CR4	D-8	R11	B-5	R55	D-7	U16	D-6	U6
C38	D-8	CR5	E-8	R12	B-6	R56	E-8	U17	D-6	U6
C39	E-8	J1	A-8	R13	B-6	R57	E-8	U18	D-7	U6
C40	F-7	J2	A-6	R14	B-6	R58	E-7	U19	E-3	U6
C41	F-7	J3	A-5	R15	B-6	R59	E-7	U20	E-4	U6
C42	F-8	J4	A-3	R16	B-6	R60	I-3	U21	E-5	U6
C43	E-7	J5	E-4	R17	B-7	R61	E-7	U22	E-5	U6
C44	H-7	J6	E-5	R18	B-7	R62	E-7	U23	E-6	U6
C45	H-7	J7	E-6	R19	B-7	R63	E-7	U24	E-6	U6
C46	H-6									

Figure 8-15. Parts Identification, Board Assembl


A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
R78
C49
C30
R42
R41
R36
C26
U61
R40
C29
L20
C28
R38
C27
R37
U68
U72
U77
U105
J8
U107
U81
U62
U65
U69
U73
U78
U82
U63
U66
U70
U74
U79
U83
C61
R35
U64
U67
C62
U71
U75
U80
U106
J9
U108
TP3
R30
R31
R34
R33
C25
R32
R39
U25
U76
C53
R28
R29
L19
U1
C63
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R71
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XA8P1
J4
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R1
C1
U19
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R2
C2
U2
C64
U11
U99
J5
U102
U28
L3
R3
C3
L4
R4
C4
U3
C65
U12
U20
U29
L5
L6
R5
C5
C50
R6
C6
U4
C66
U13
J3
L7
R7
U100
J6
U103
U30
L8
C7
U21
L9
R8
C8
U5
C67
U14
U31
R9
C9
L10
R10
C10
U6
C68
U15
U22
C51
L11
L12
R11
C11
U32
TP4
C72
J2
L13
R12
C12
U7
C69
U16
U23
U33
C46
L14
R13
C13
R69
L15
R14
C14
U8
C70
U17
U101
J7
U104
U34
U5
L16
R15
C15
R67
R25
C23
C24
L17
R16
U24
C45
C16
U9
C71
U18
C14
L18
R17
C17
U47
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R66
C77
C78
R18
C33
R49
C18
C55
U27
U26
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R48
U52
R72
L21
L22
R73
R68
C48
R19
C31
U41
R44
R55
C47
C76
R43
R27
R50
R70
S1
J1
R26
R74
C75
C34
U5
R22
TP1
R21
U42
U43
U44
U45
U46
R20
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CR4
C35
R52
C38
R56
CR5
C39
R45
R57
C42
CR1
C32
R46
C37
R54
R53
R61
R63
C43
R62
R58
R59
C41
C40
C54
CR2
R47
CR3
R24
C22
C21
U48
C20
C19
R23

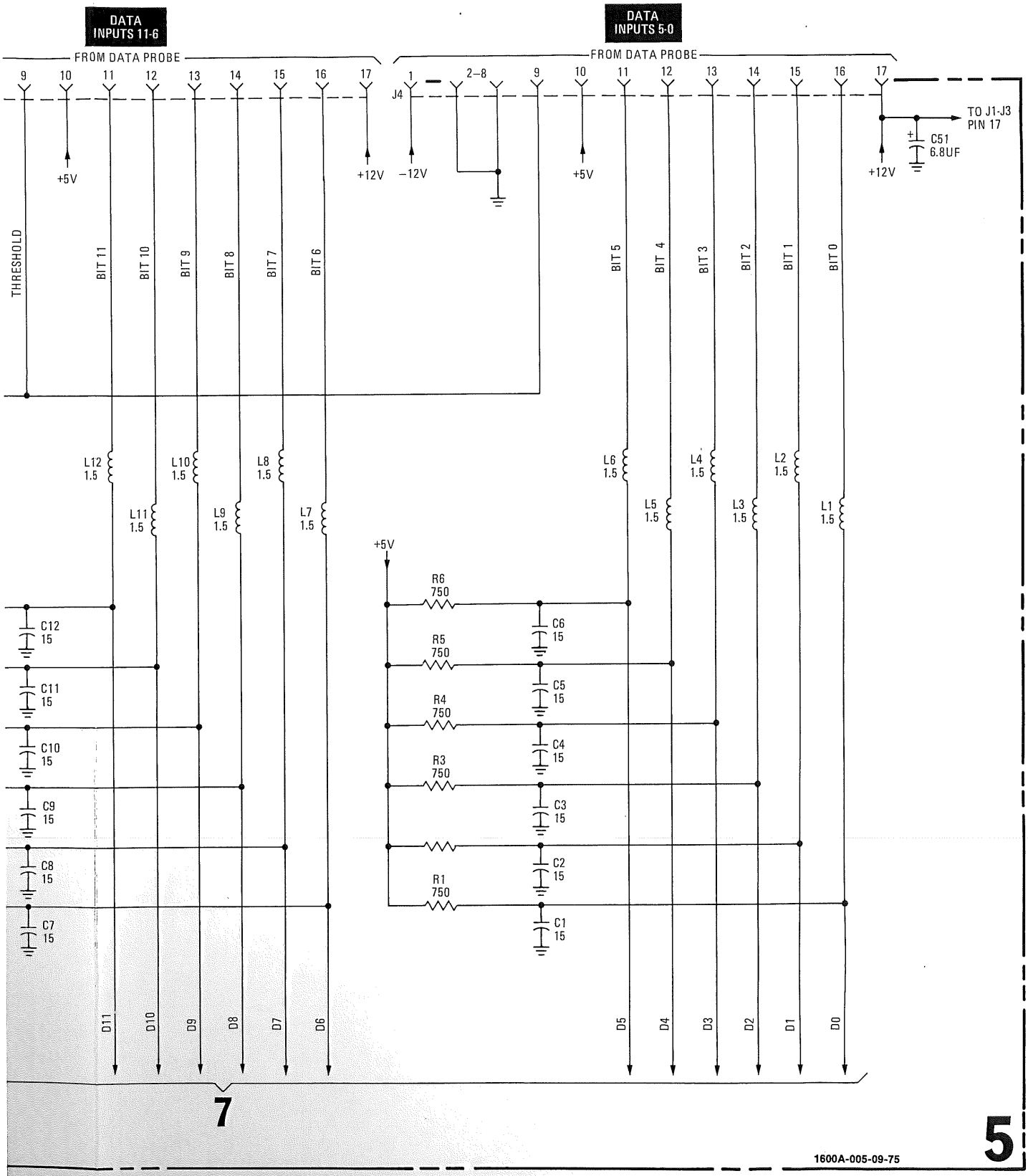
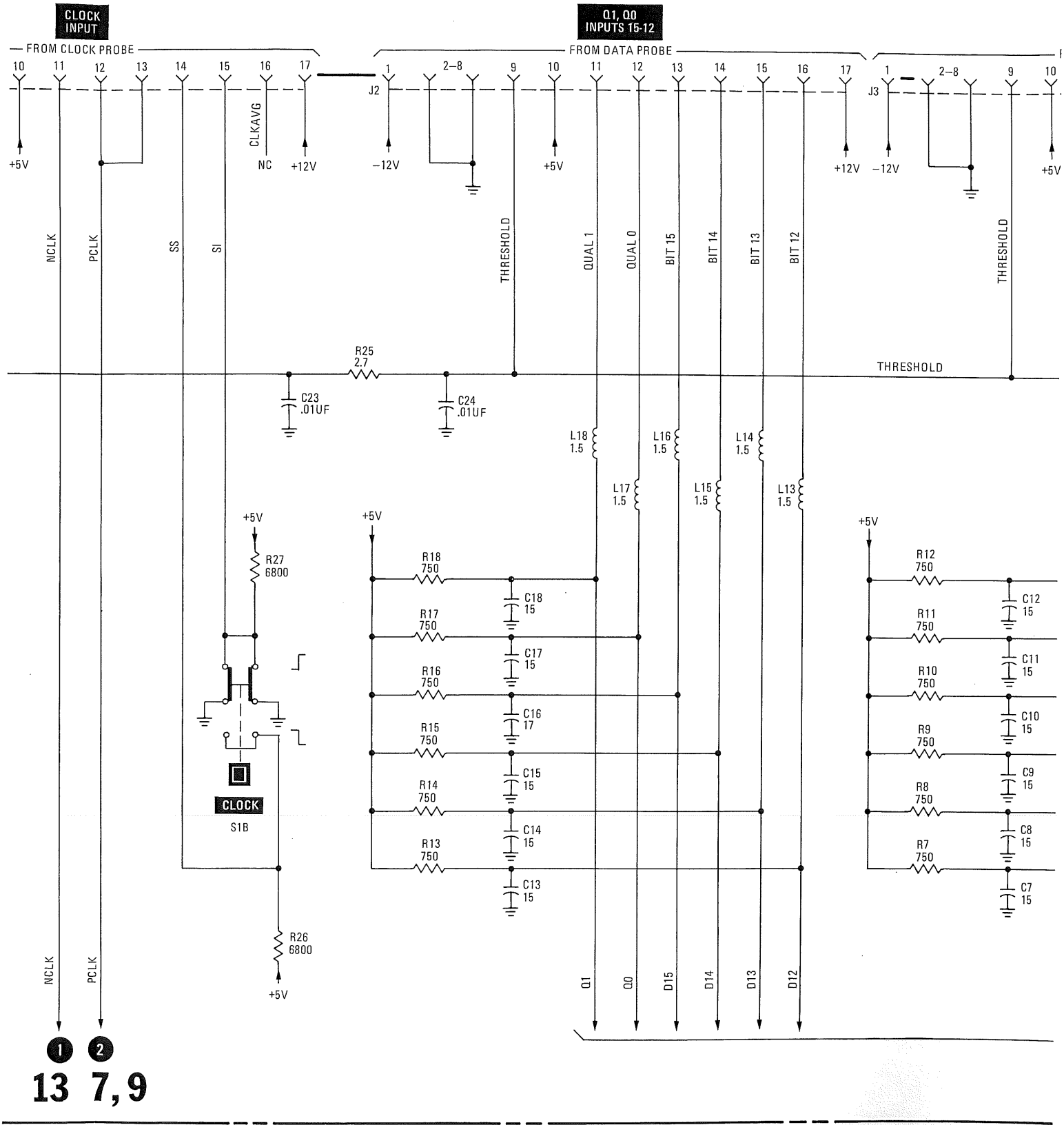
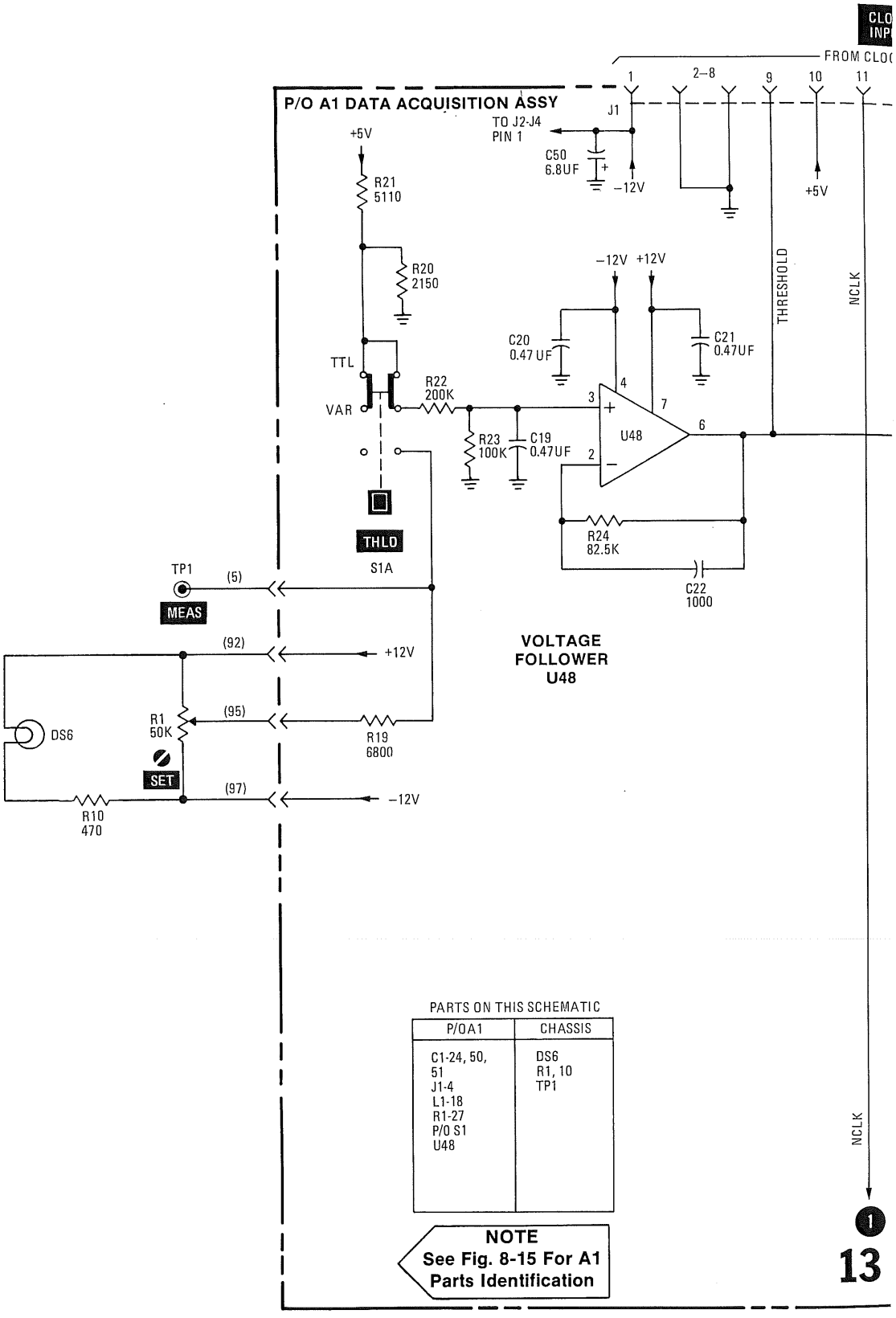


Figure 8-16.
Schematic 5, Data Input and Threshold


CLOCK INPUT
FROM CLOCK PROBE
Q1, Q0 INPUTS 15-12
FROM DATA PROBE
J2
J3
CLKAVG
NC
+5V
+12V
−12V
NCLK
PCLK
SS
SI
THRESHOLD
QUAL 1
QUAL 0
BIT 15
BIT 14
BIT 13
BIT 12
R25 2.7
C23 .01UF
C24 .01UF
R27 6800
R26 6800
CLOCK
S1B
L18 1.5
L17 1.5
L16 1.5
L15 1.5
L14 1.5
L13 1.5
R18 750
R17 750
R16 750
R15 750
R14 750
R13 750
C18 15
C17 15
C16 17
C15 15
C14 15
C13 15
R12 750
R11 750
R10 750
R9 750
R8 750
R7 750
C12 15
C11 15
C10 15
C9 15
C8 15
C7 15
Q1
Q0
D15
D14
D13
D12
1
2
13
7,9


P/O A1 DATA ACQUISITION ASSY
FROM CLOC
1
2–8
9
10
11
J1
TO J2-J4
PIN 1
+5V
C50
6.8UF
–12V
+5V
R21
5110
R20
2150
–12V
+12V
C20
0.47 UF
C21
0.47UF
THRESHOLD
NCLK
TTL
VAR
R22
200K
R23
100K
C19
0.47UF
U48
THLD
S1A
R24
82.5K
C22
1000
TP1
(5)
MEAS
(92)
+12V
VOLTAGE
FOLLOWER
U48
DS6
R1
50K
SET
(95)
R19
6800
(97)
–12V
R10
470
PARTS ON THIS SCHEMATIC
P/OA1
CHASSIS
C1-24, 50, 51
J1-4
L1-18
R1-27
P/O S1
U48
DS6
R1, 10
TP1
NOTE
See Fig. 8-15 For A1
Parts Identification
NCLK
1

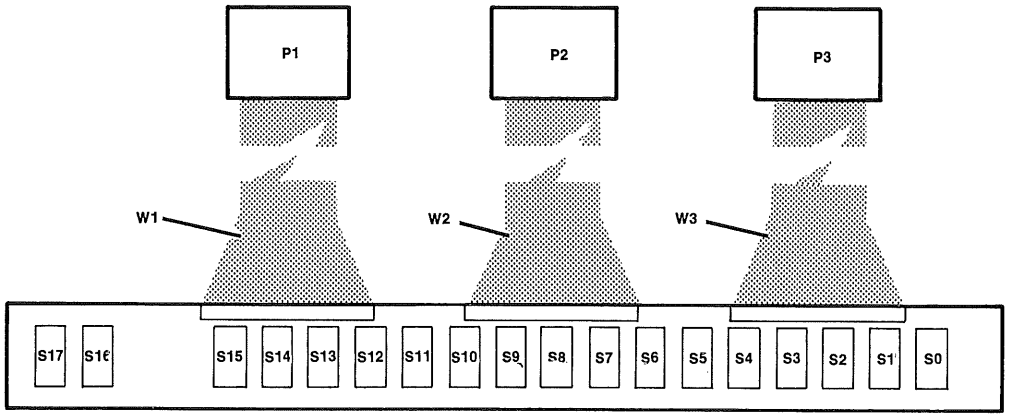


Figure 8-17. Parts Identification, Board Assembly A6

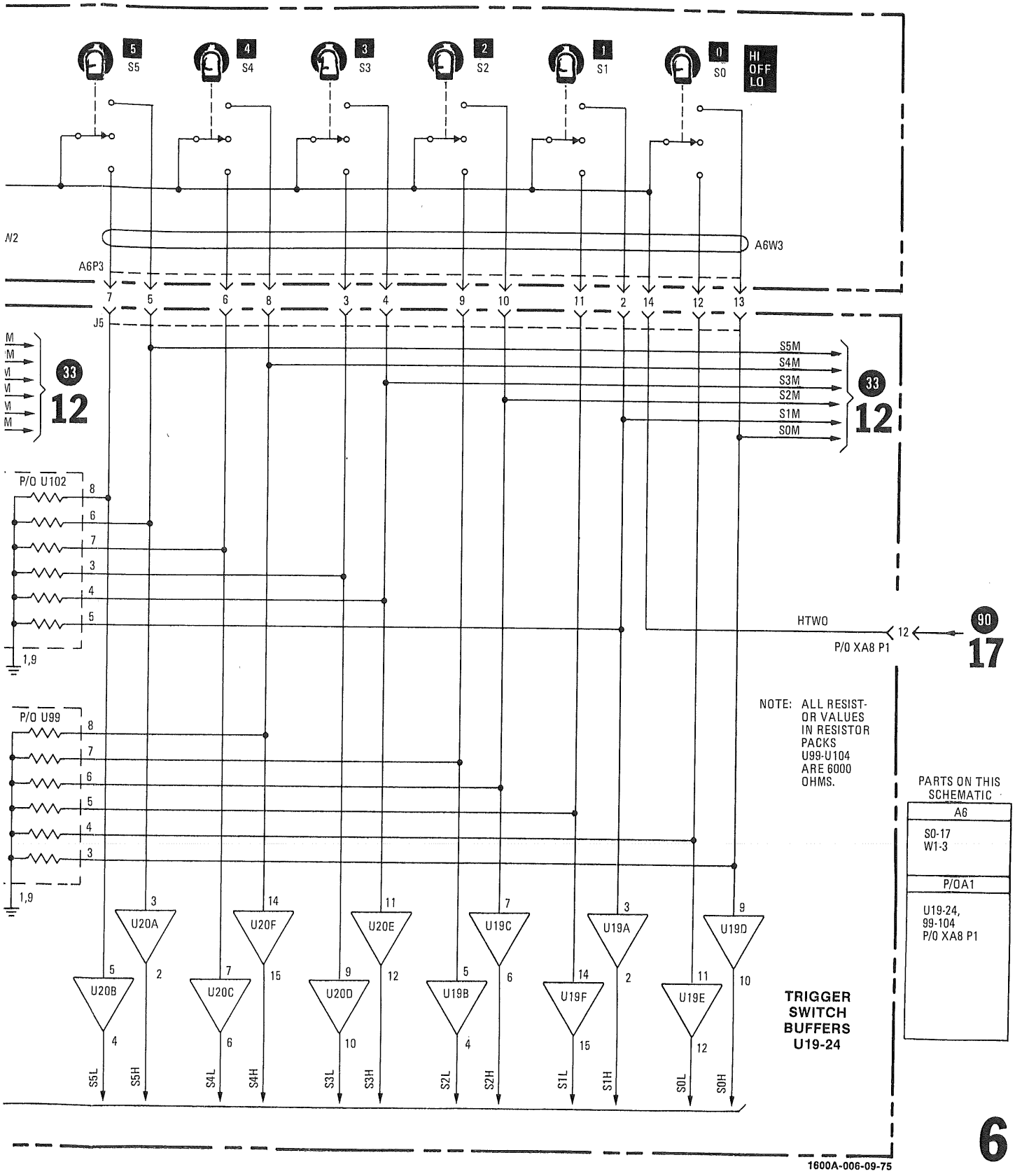
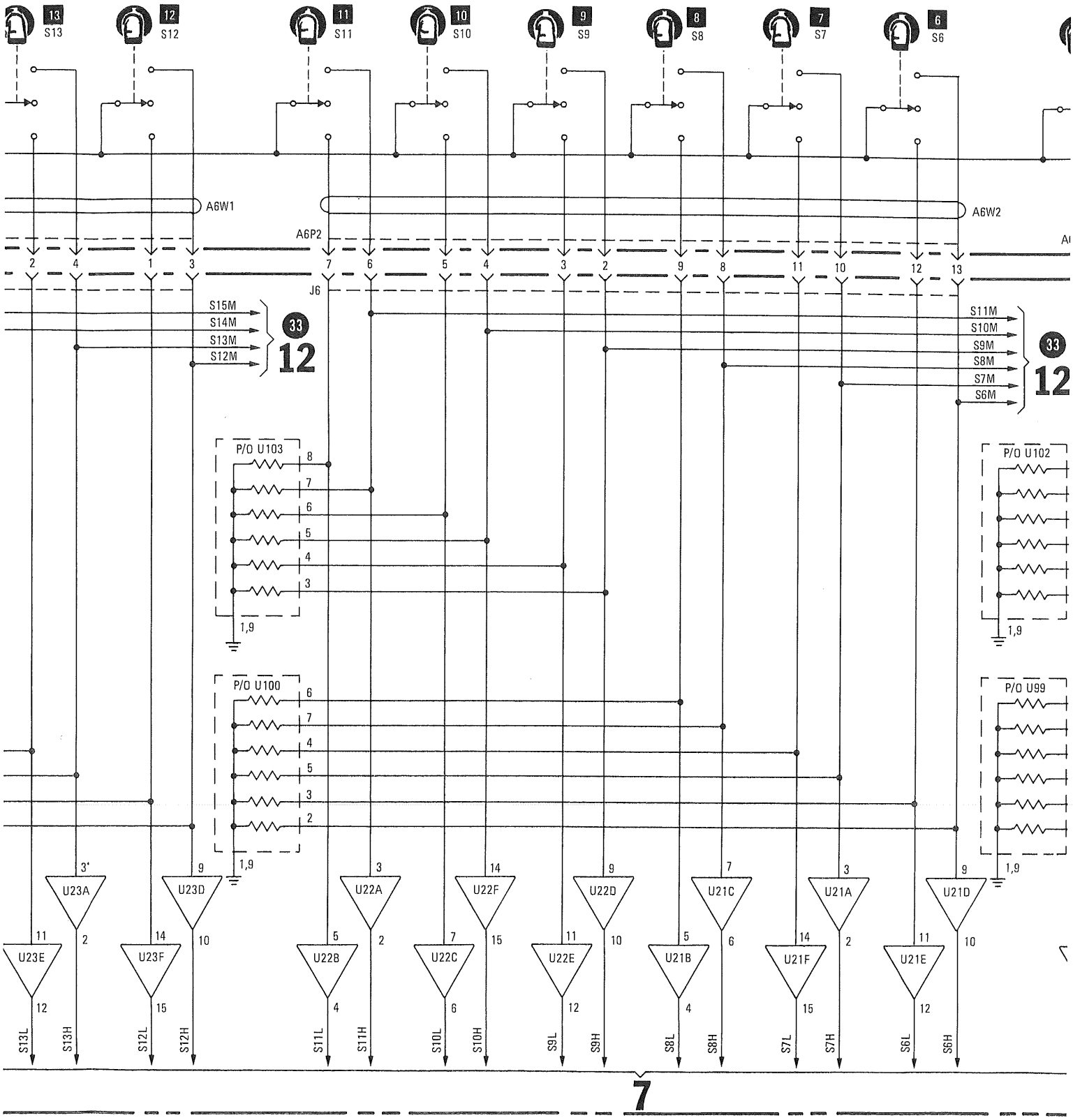
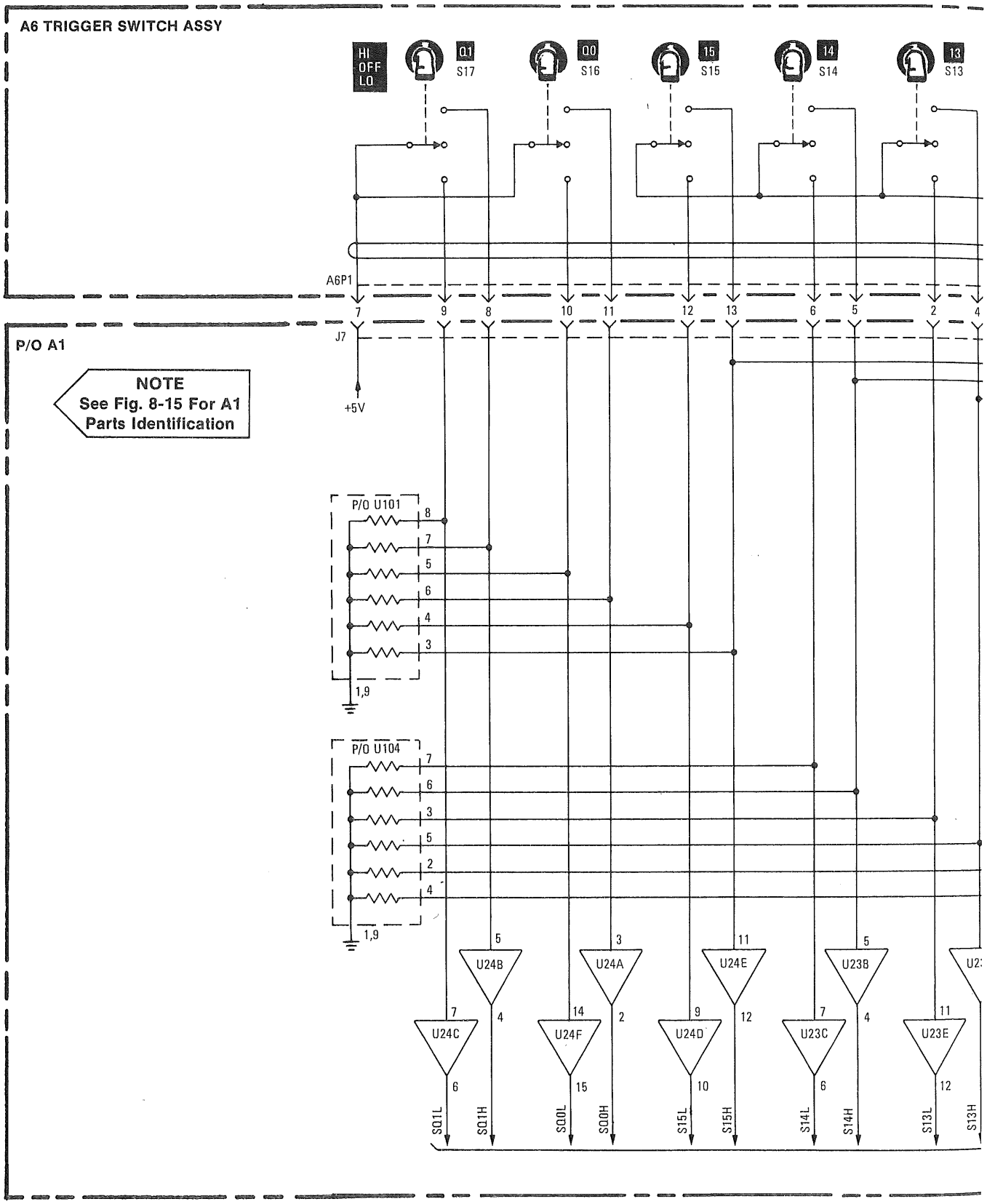


Figure 8-18.
Schematic 6, Trigger Word Select
8-21/(8-22 blank)


13 S13
12 S12
11 S11
10 S10
9 S9
8 S8
7 S7
6 S6
A6W1
A6W2
A6P2
J6
S15M
S14M
S13M
S12M
S11M
S10M
S9M
S8M
S7M
S6M
33
12
P/O U103
P/O U102
P/O U100
P/O U99
1,9
U23A
U23D
U23E
U23F
U22A
U22B
U22C
U22D
U22E
U22F
U21A
U21B
U21C
U21D
U21E
U21F
S13L
S13H
S12L
S12H
S11L
S11H
S10L
S10H
S9L
S9H
S8L
S8H
S7L
S7H
S6L
S6H


A6 TRIGGER SWITCH ASSY
HI
OFF
LO
Q1
S17
Q0
S16
15
S15
14
S14
13
S13
A6P1
7
9
8
10
11
12
13
6
5
2
4
J7
+5V
P/O A1
NOTE
See Fig. 8-15 For A1
Parts Identification
P/O U101
8
7
5
6
4
3
1,9
P/O U104
7
6
3
5
2
4
1,9
U24B
U24A
U24E
U23B
U24C
U24F
U24D
U23C
U23E
SQ1L
SQ1H
SQ0L
SQ0H
S15L
S15H
S14L
S14H
S13L
S13H

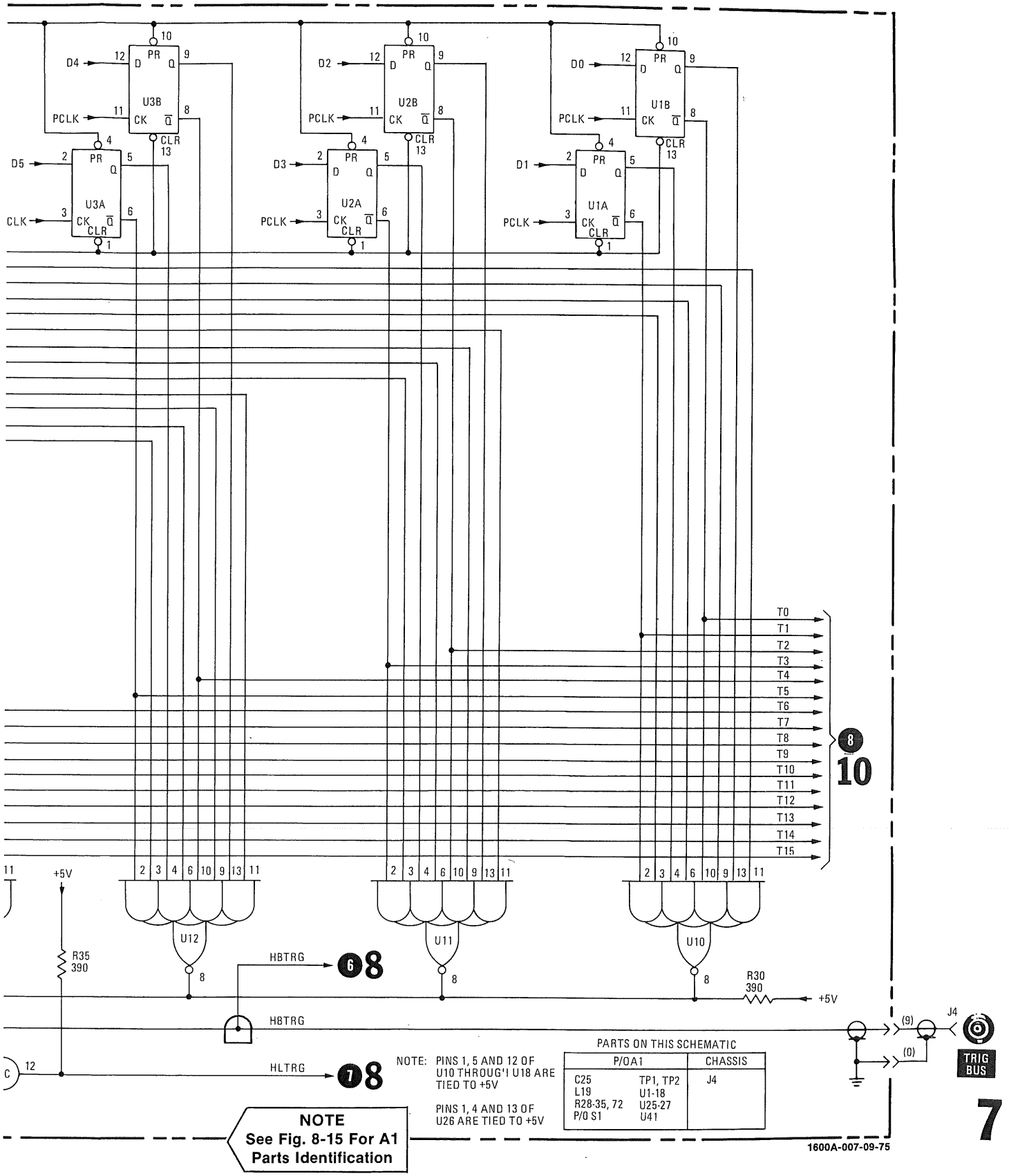
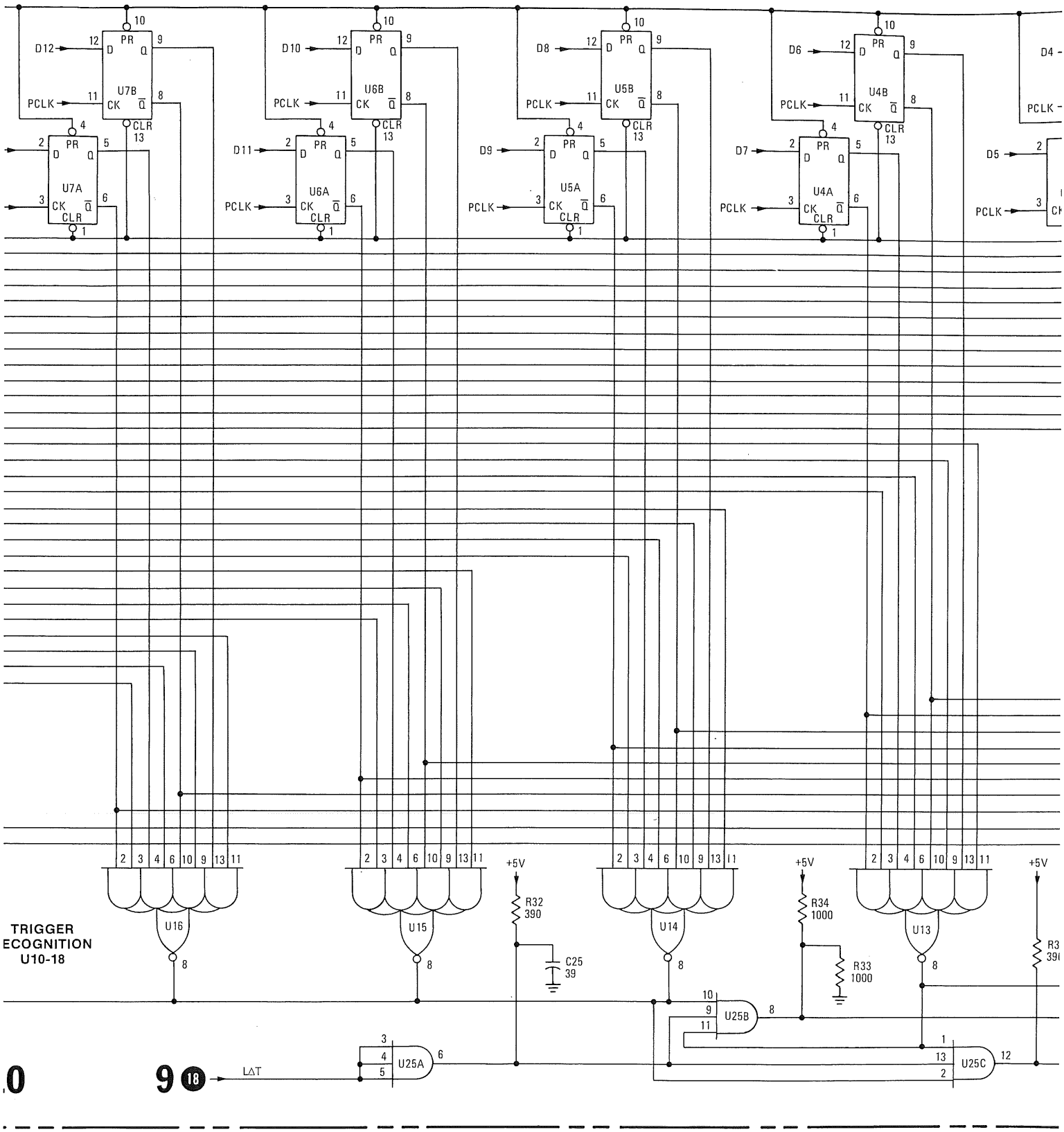
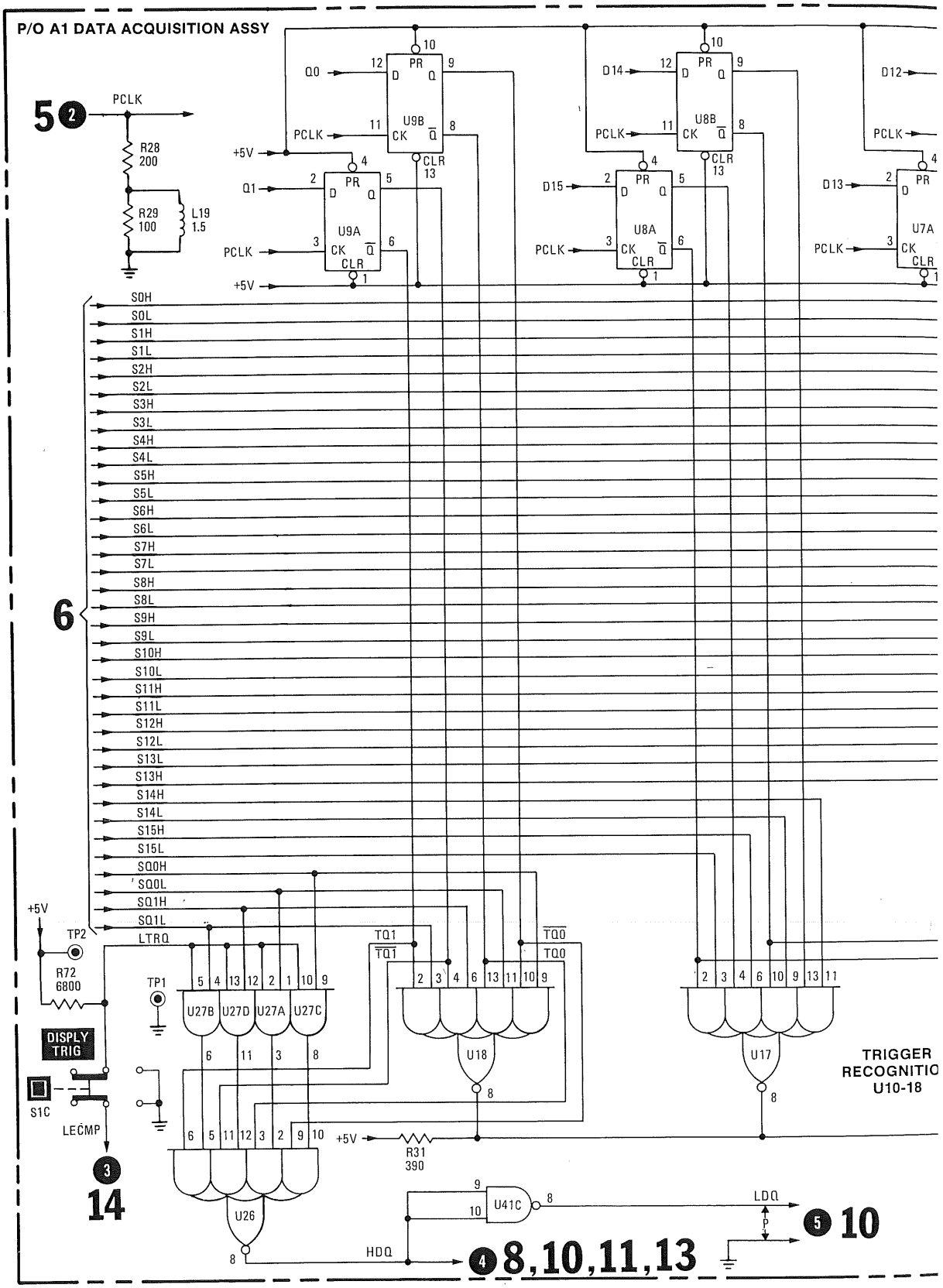


Figure 8-19.
Schematic 7, Temporary Storage and Pattern Recognition


D12
D10
D8
D6
D4
D11
D9
D7
D5
PCLK
U7B
U6B
U5B
U4B
U7A
U6A
U5A
U4A
PR
CLR
U16
U15
U14
U13
+5V
R32
390
C25
39
R34
1000
R33
1000
U25B
U25A
U25C
LAT
TRIGGER
ECOGNITION
U10-18


P/O A1 DATA ACQUISITION ASSY
PCLK
R28 200
R29 100
L19 1.5
+5V
U9B
U9A
U8B
U8A
U7A
Q0
Q1
D14
D15
D12
D13
CLR
S0H
S0L
S1H
S1L
S2H
S2L
S3H
S3L
S4H
S4L
S5H
S5L
S6H
S6L
S7H
S7L
S8H
S8L
S9H
S9L
S10H
S10L
S11H
S11L
S12H
S12L
S13L
S13H
S14H
S14L
S15H
S15L
SQ0H
SQ0L
SQ1H
SQ1L
LTRQ
TP2
R72 6800
TP1
DISPLY TRIG
S1C
LECMP
U27B
U27D
U27A
U27C
U26
U18
U17
TQ1
TQ0
R31 390
U41C
LDQ
HDQ
TRIGGER RECOGNITIO
U10-18
14
10
8,10,11,13

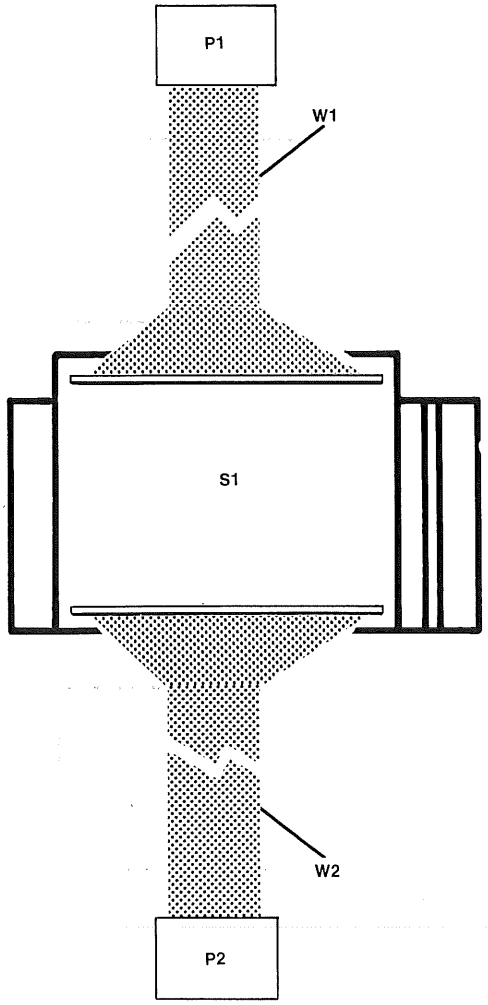
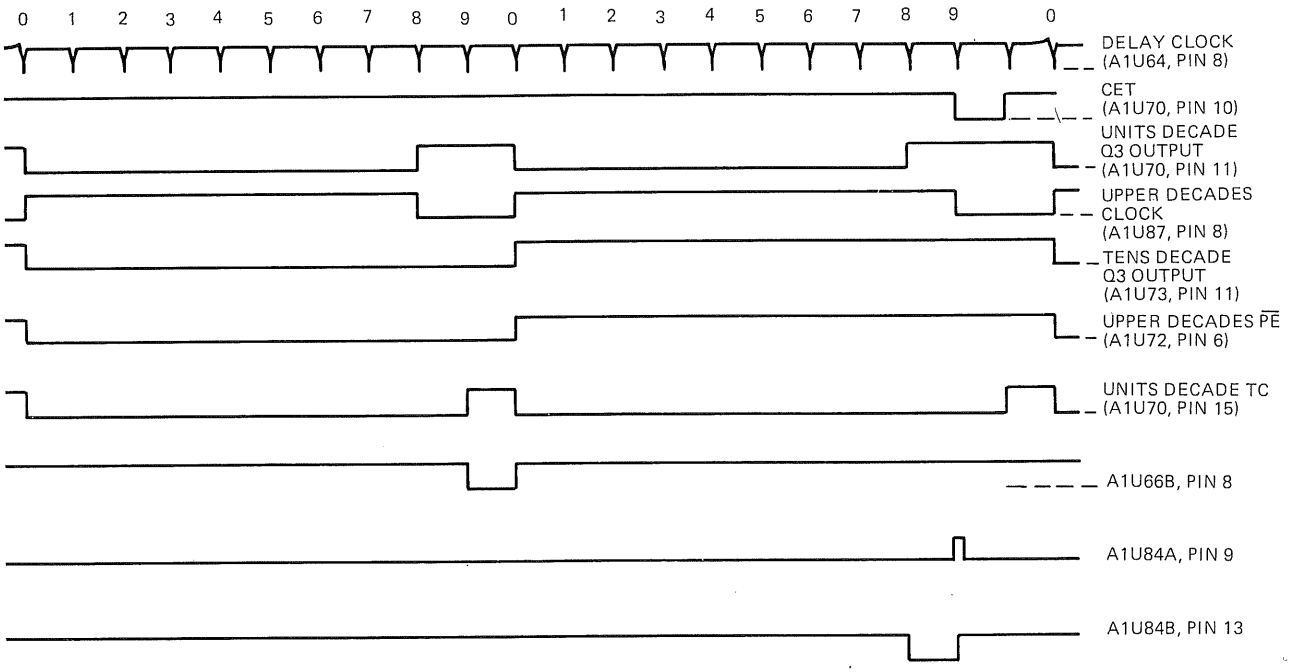


Figure 8-20. Parts Identification, Board Assembly A10

DIGITAL DELAY TIMING DIAGRAM
SCHEMATIC 8

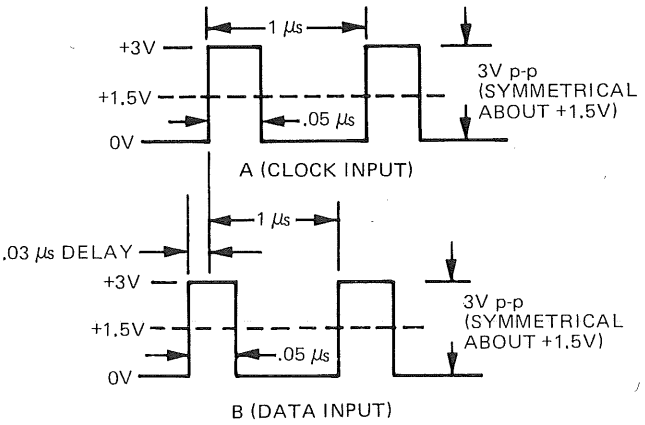


1. Connect test equipment as shown for Operational Check Test Setup in Section V.

2. Set Model 1600A controls as follows:

CLOCK	⌐
THLD	TTL
QUALIFIER Q1, Q0	OFF
SAMPLE MODE	REPET
START DSPL	ON
TRIGGER MODE	
NORM/ARM	NORM
LOCAL/BUS	LOCAL
WORD	ON
TRIGGER WORD	All Switches HI
DELAY ON/OFF	ON
DELAY Thumbwheels	00020
DISPLAY MODE	TABLE A

3. Apply waveforms shown below to clock and data inputs.



NOTE

1. Unused logic not shown for A1U64, U65, U77, U81, and U87.

U67B/U84A and B* TRUTH TABLE

J	$\overline{K}$	Q	$\overline{Q}$
L	H	NO	CHANGE
L	L	L	H
H	L	H	L

* U67A and U71A/B are wired D Flip-Flops

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Figure 8-21. Schematic 8, Digital Delay and Trigger Generator (Sheet 1 of 2)

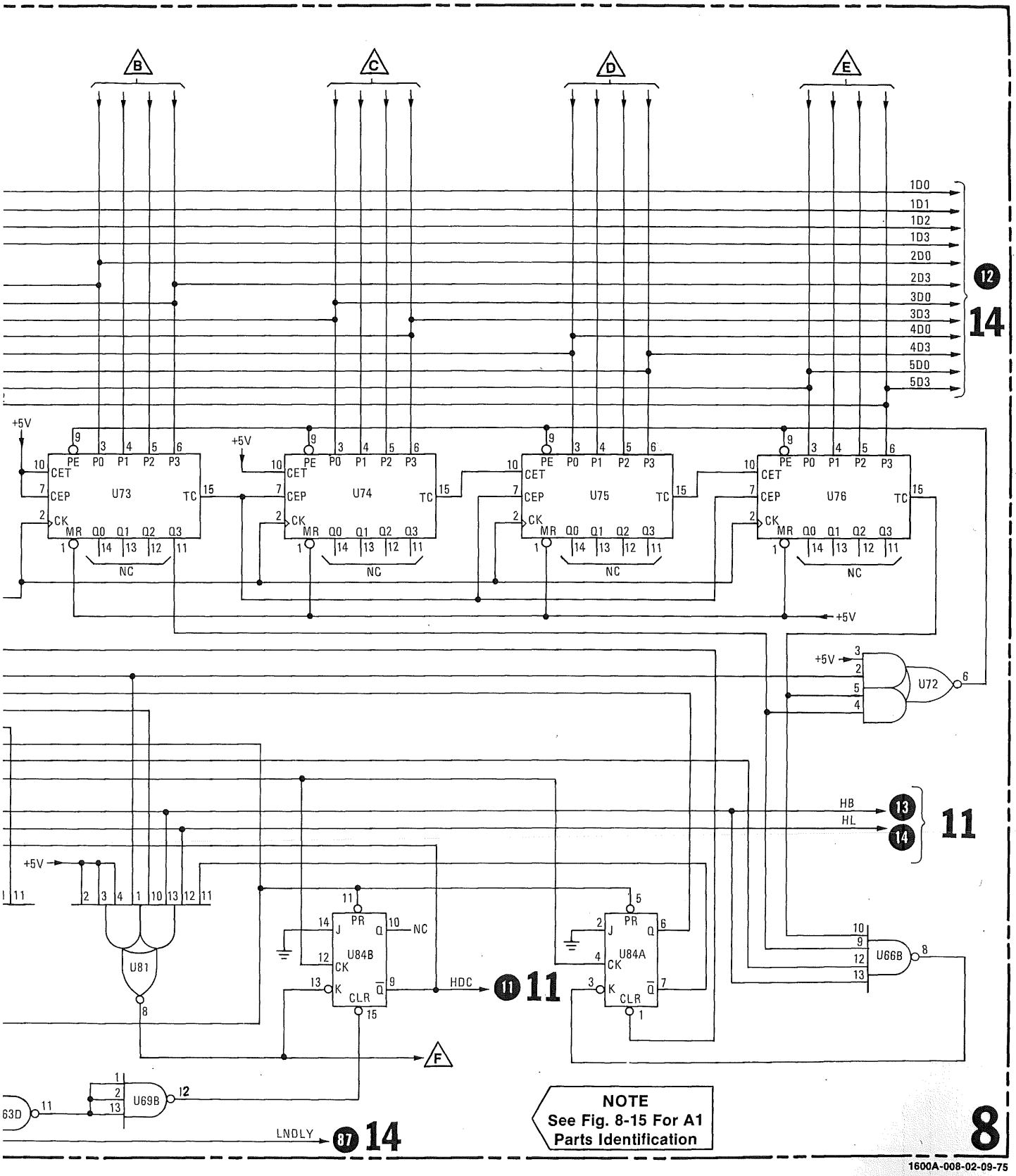
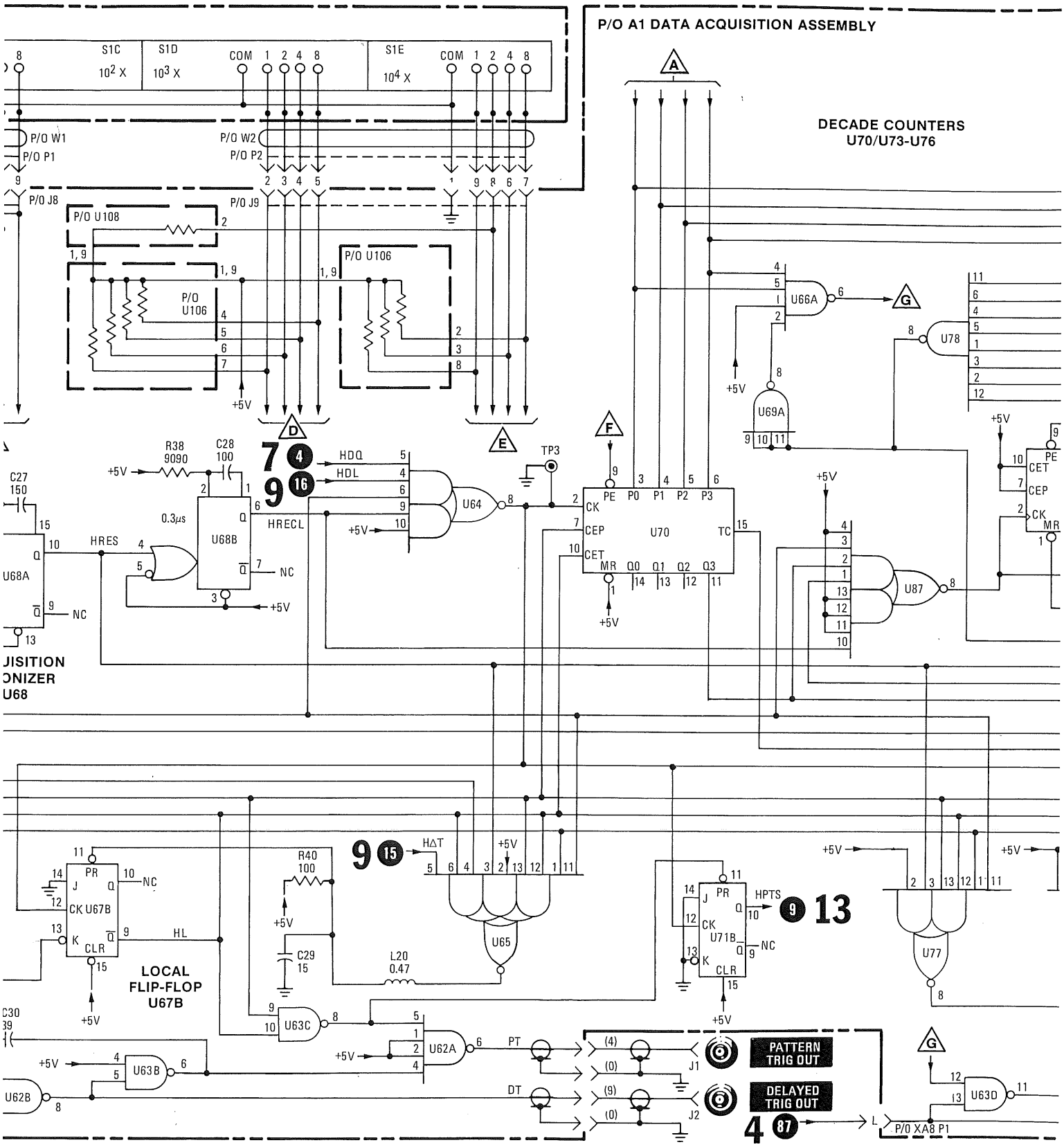
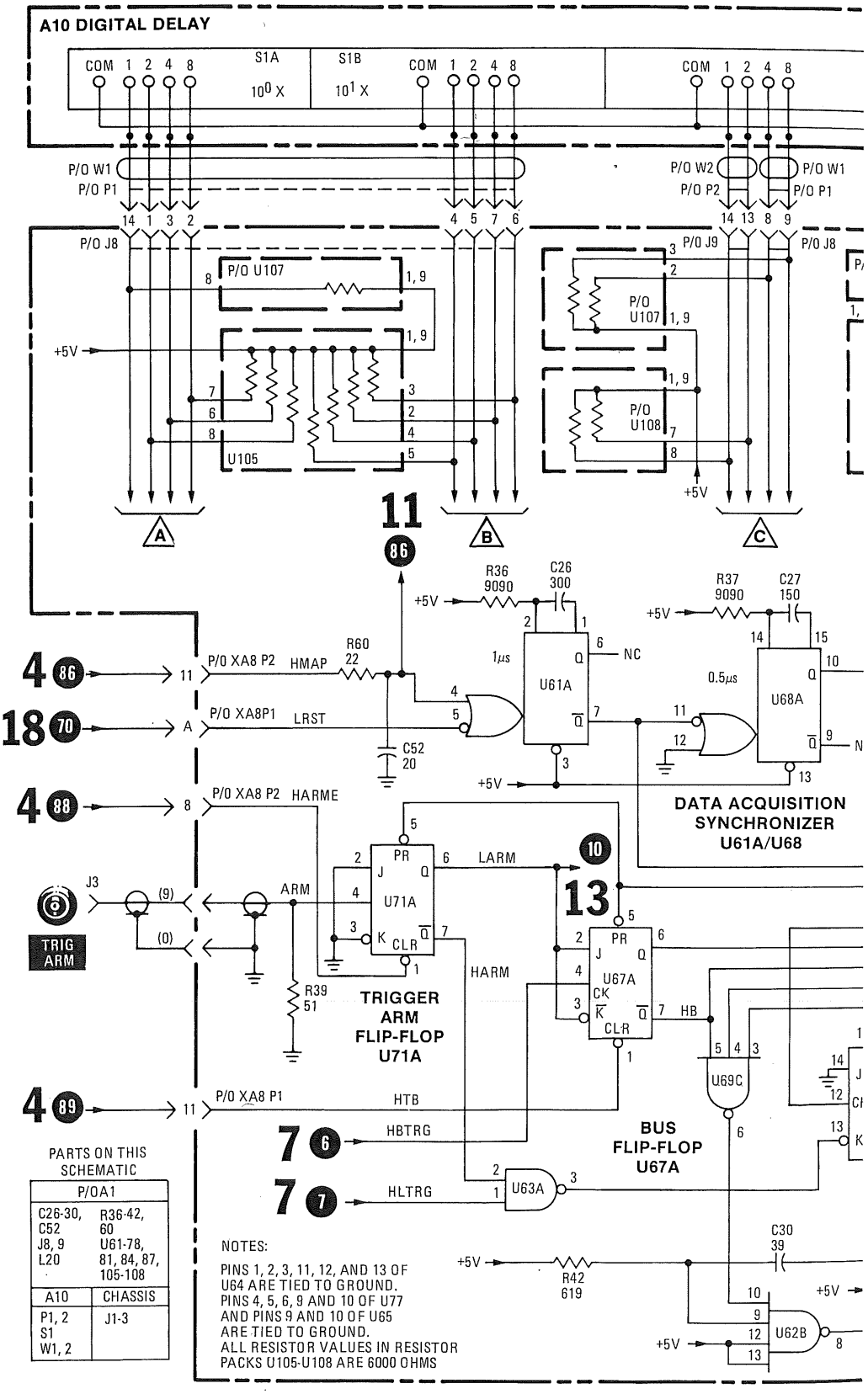


Figure 8-21.
Schematic 8, Digital Delay and Trigger Generator (Sheet 2 of 2)


P/O A1 DATA ACQUISITION ASSEMBLY
DECADE COUNTERS
U70/U73-U76
S1C
10^2 X
S1D
10^3 X
S1E
10^4 X
COM 1 2 4 8
P/O W1
P/O P1
P/O W2
P/O P2
P/O J8
P/O J9
P/O U108
P/O U106
+5V
U66A
U69A
U78
U64
U70
U87
U68B
U68A
R38 9090
C28 100
C27 150
0.3μs
HRES
HRECL
HDQ
HDL
TP3
NC
U63C
U63B
U62A
U62B
U65
U71B
U77
R40 100
C29 15
L20 0.47
C30 39
HΔT
HPTS
HL
LOCAL FLIP-FLOP U67B
PATTERN TRIG OUT
DELAYED TRIG OUT
PT
DT
J1
J2
P/O XA8 P1
U63D



PARTS ON THIS SCHEMATIC

P/OA1	
C26-30, C52 J8, 9 L20	R36-42, 60 U61-78, 81, 84, 87, 105-108
A10	CHASSIS
P1, 2 S1 W1, 2	J1-3

NOTES:

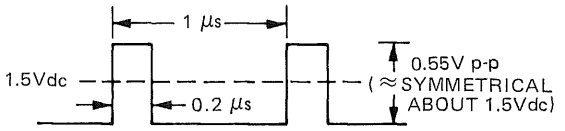
PINS 1, 2, 3, 11, 12, AND 13 OF U64 ARE TIED TO GROUND.
PINS 4, 5, 6, 9 AND 10 OF U77 AND PINS 9 AND 10 OF U65 ARE TIED TO GROUND.
ALL RESISTOR VALUES IN RESISTOR PACKS U105-U108 ARE 6000 OHMS

TIMING GENERATOR TIMING DIAGRAM
SCHEMATIC 9

1. Set Model 1600A controls as follows.

CLOCK	⌐¬
THLD	TTL
START DSPL	ON
WORD	ON
QUALIFIER	
DSPLY/TRIG	TRIG
Q1, Q0	OFF
TRIGGER WORD	Bits 0-15 OFF

2. Connect HP Model 8013B Pulse Generator OUTPUT (+) connector to CLOCK probe and apply waveform below.



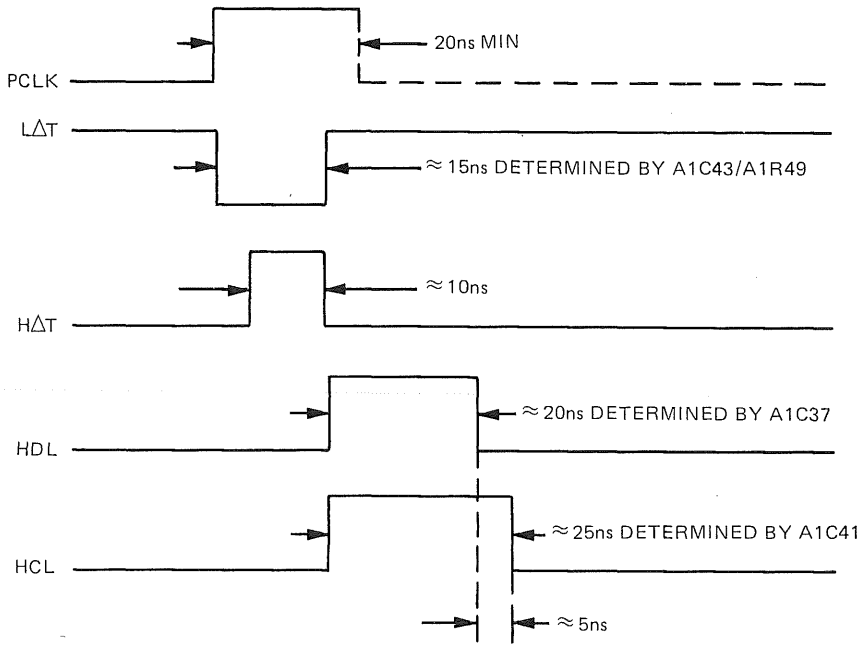


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Figure 8-22. Schematic 9, Timing Generator (Sheet 1 of 2)

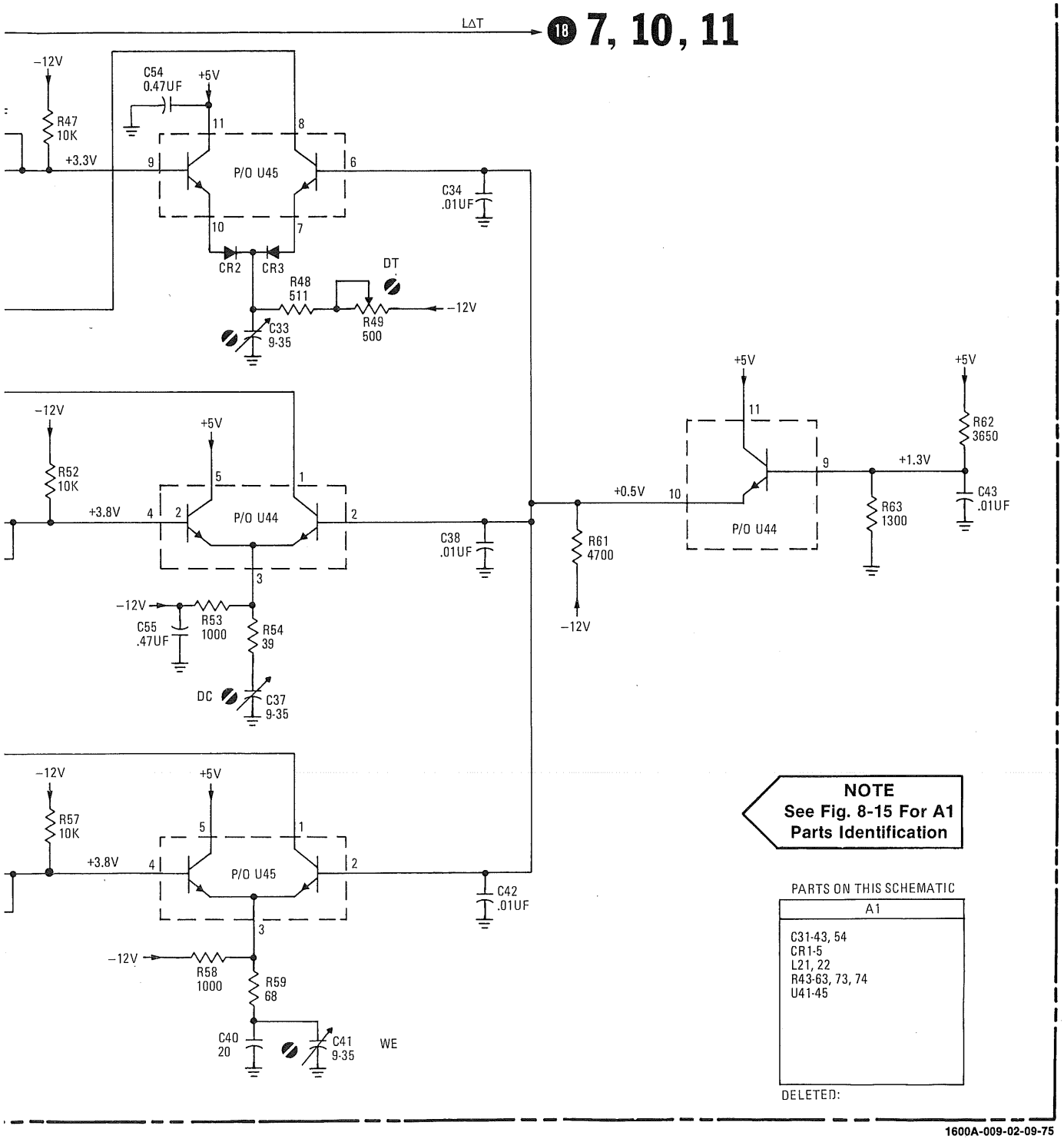
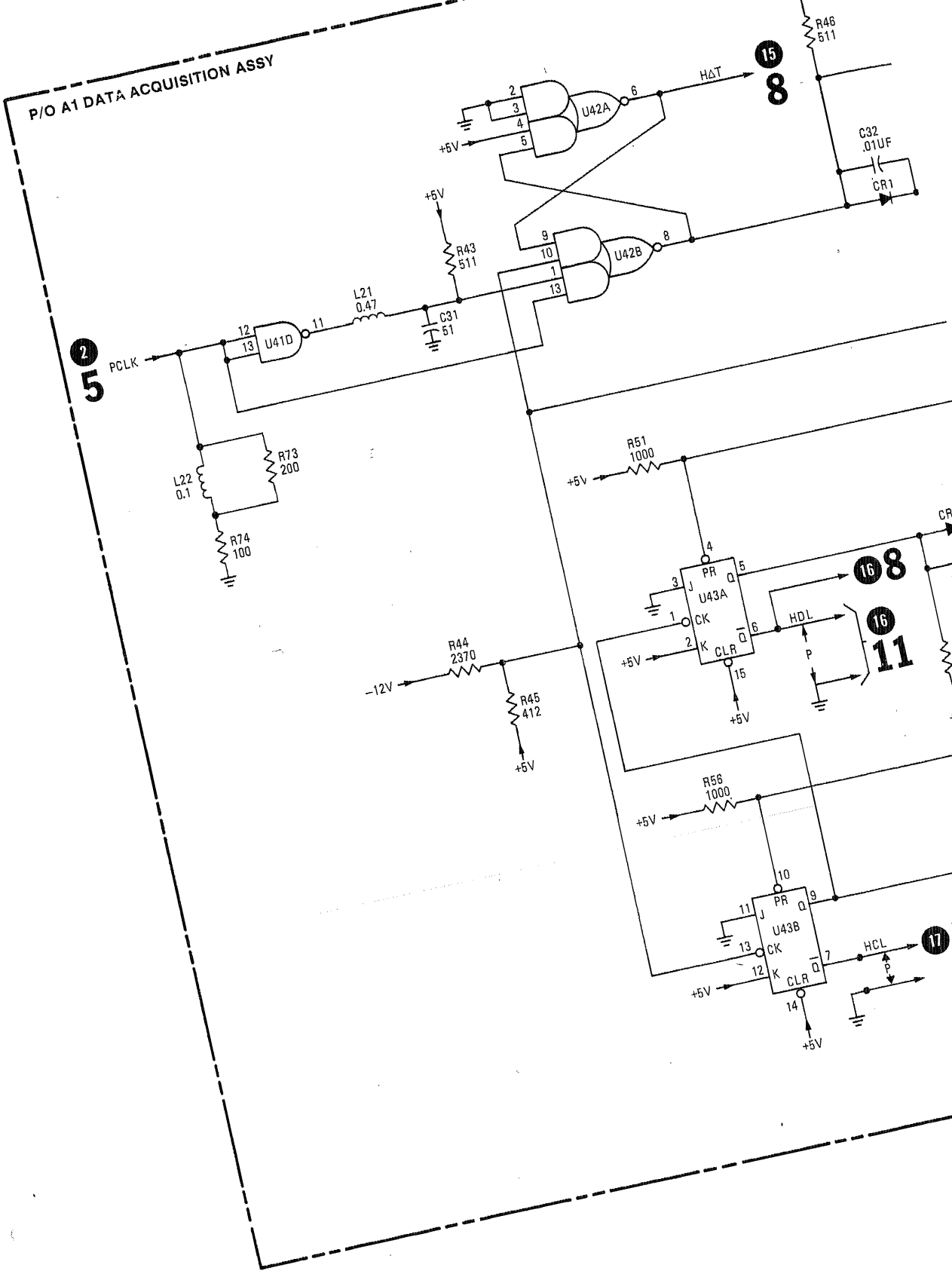


Figure 8-22.
Schematic 9, Timing Generator (Sheet 2 of 2)


P/O A1 DATA ACQUISITION ASSY
R46
511
HΔT
15
8
U42A
+5V
C32
.01UF
CR1
R43
511
U42B
L21
0.47
C31
51
U41D
2
5
PCLK
L22
0.1
R73
200
R74
100
R51
1000
U43A
PR
CK
CLR
HDL
16
8
16
11
R44
2370
R45
412
−12V
R56
1000
U43B
HCL
17
P

MEMORY WRITE TIMING DIAGRAM
SCHEMATIC 10

Set up Model 1600A as follows:

1. Connect Test Equipment as shown for Operational Check Test Setup in Section V.

2. Set Model 1600A controls as follows.

CLOCK	⌐¬
THLD	TTL
QUALIFIER Q0/Q1	HI
DSPLY/TRIG	TRIG
SAMPLE MODE	REPET
TRIGGER MODE	
START DSPL	ON
NORM/ARM	NORM
LOCAL/BUS	LOCAL
WORK	ON
TRIGGER WORD	All Switches HI

CAUTION

A1U28 through A1U34, and A1U39 are CMOS devices which are easily damaged if contacted by static voltages.

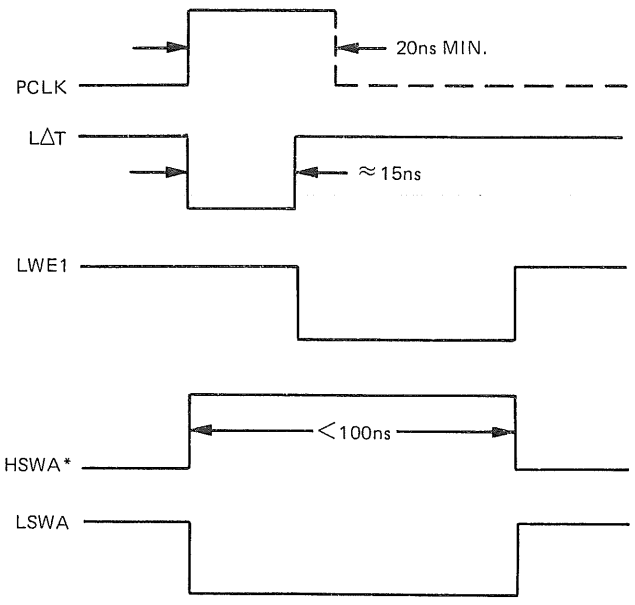


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Figure 8-23. Schematic 10, A-memory (Sheet 1 of 2)

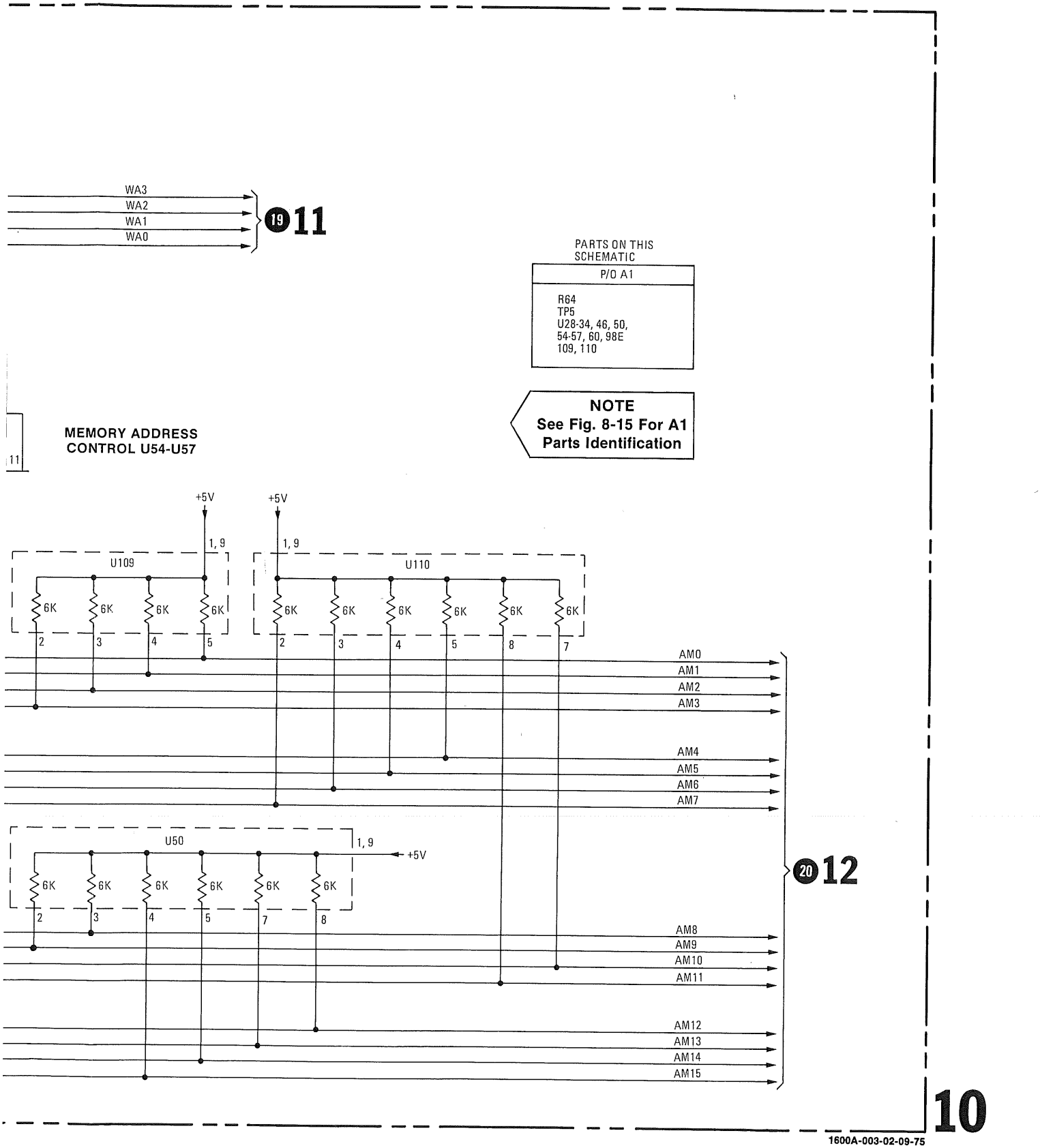
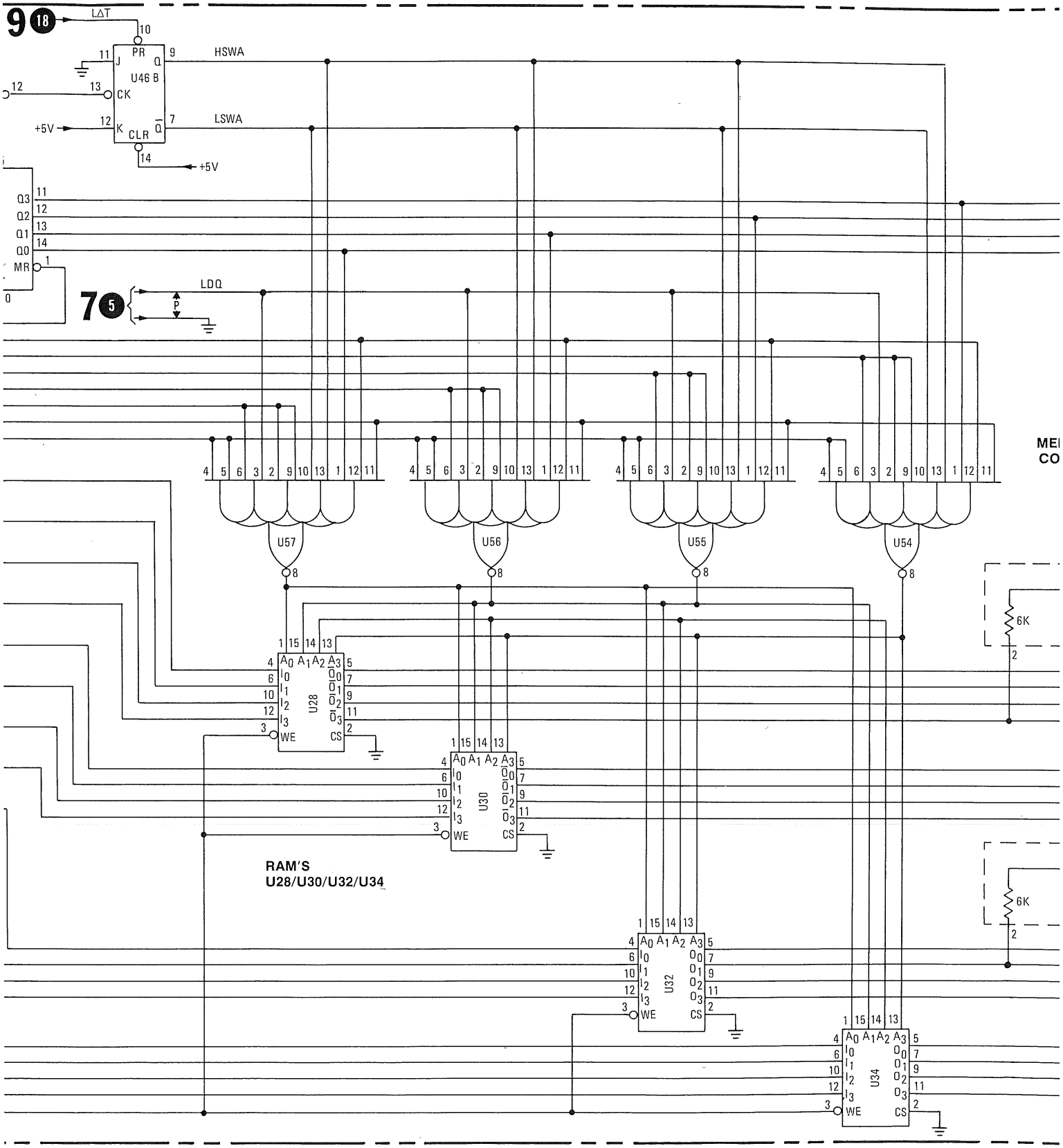
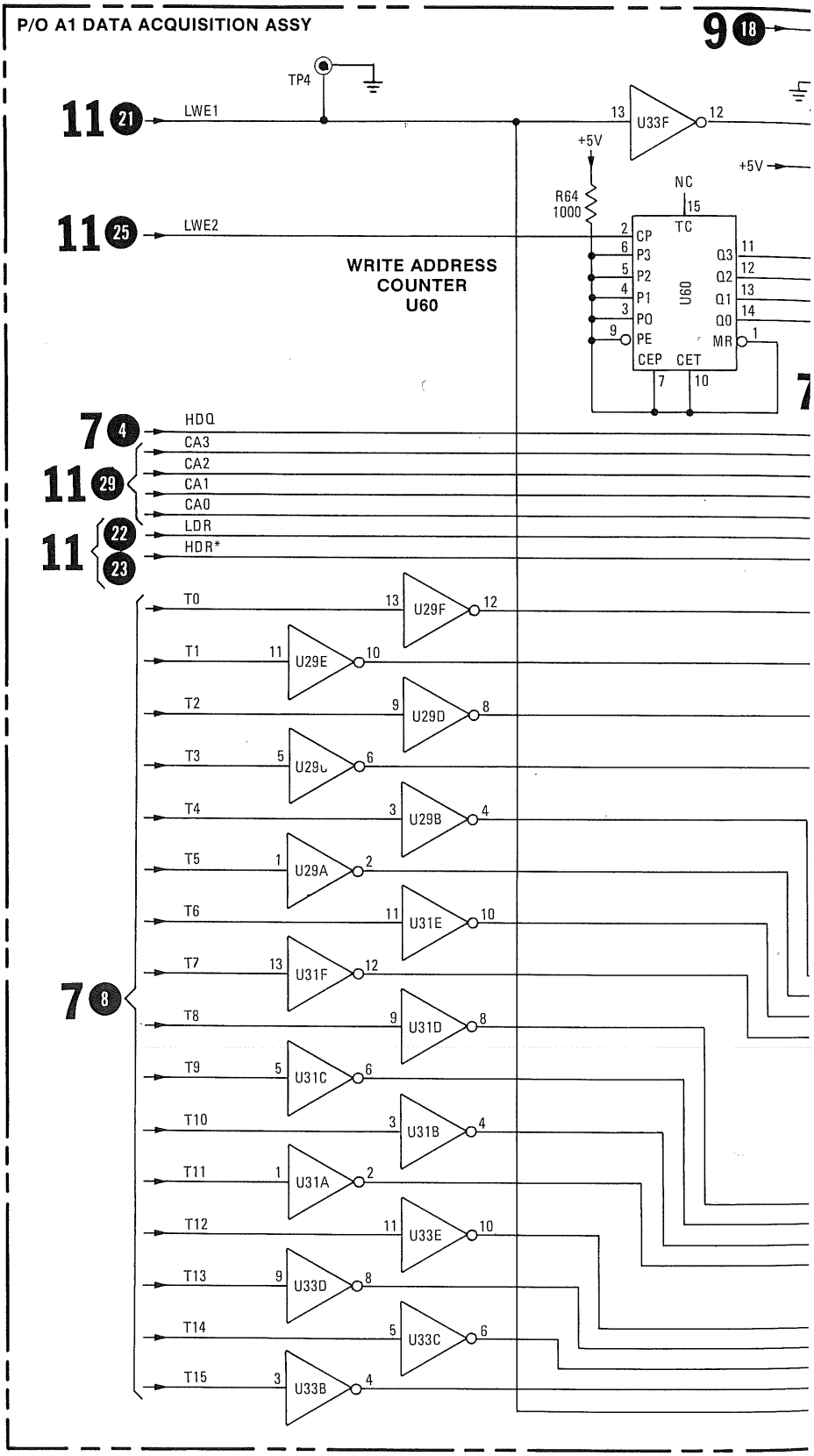


Figure 8-23.
Schematic 10, A-memory (Sheet 2 of 2)


LΔT
HSWA
LSWA
+5V
LDQ
MR
U46 B
PR
CK
CLR
U57
U56
U55
U54
U28
U30
U32
U34
WE
CS
6K
RAM'S
U28/U30/U32/U34


P/O A1 DATA ACQUISITION ASSY
9 18
TP4
11 21 LWE1
11 25 LWE2
WRITE ADDRESS COUNTER U60
+5V
R64 1000
NC
15
TC
U60
CP
P3
P2
P1
PO
PE
CEP
CET
Q3
Q2
Q1
Q0
MR
7 4 HDQ
CA3
CA2
11 29 CA1
CA0
LDR
11 22
HDR*
23
T0 U29F
T1 U29E
T2 U29D
T3 U29C
T4 U29B
T5 U29A
T6 U31E
T7 U31F
7 8
T8 U31D
T9 U31C
T10 U31B
T11 U31A
T12 U33E
T13 U33D
T14 U33C
T15 U33B

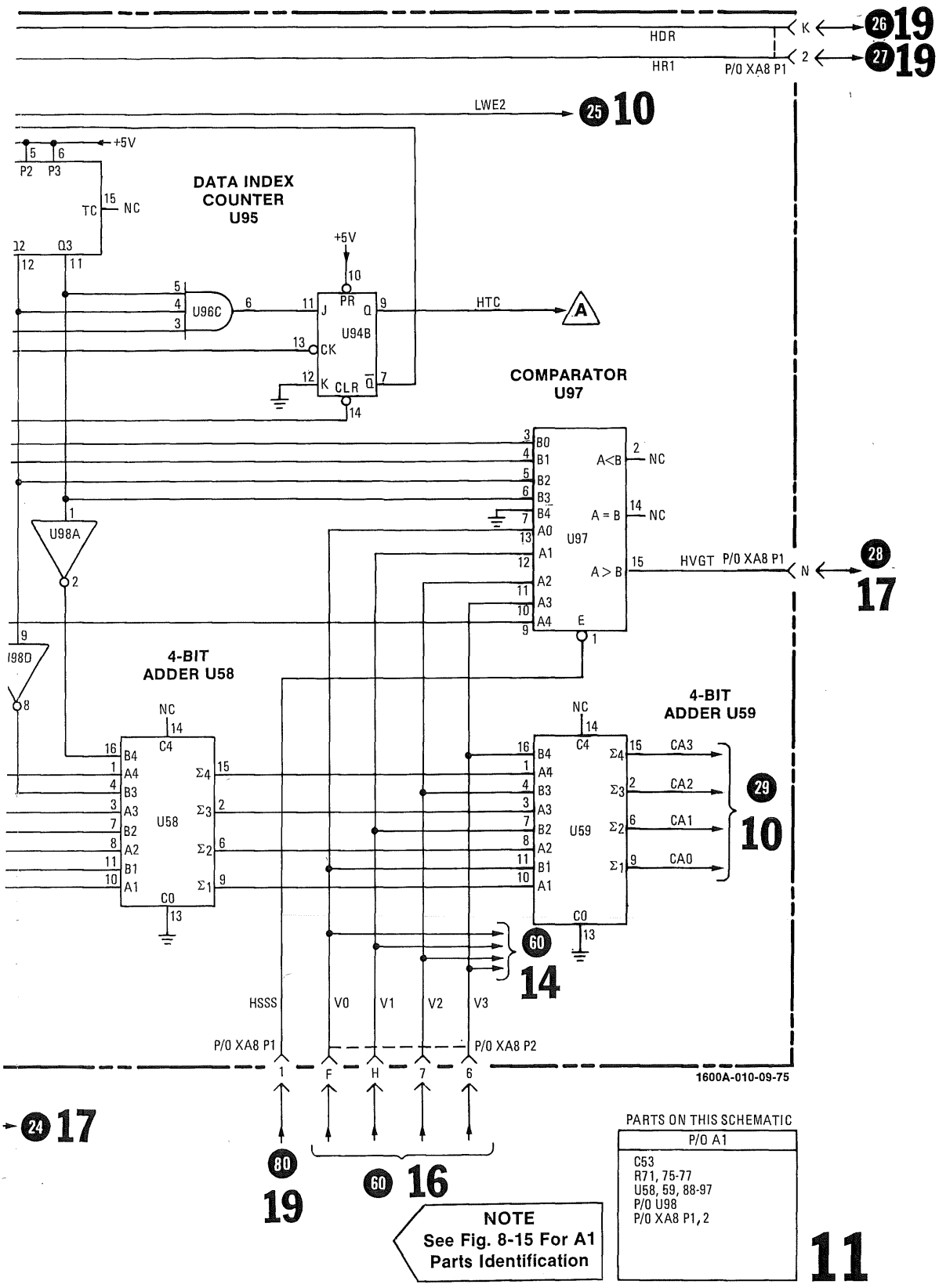
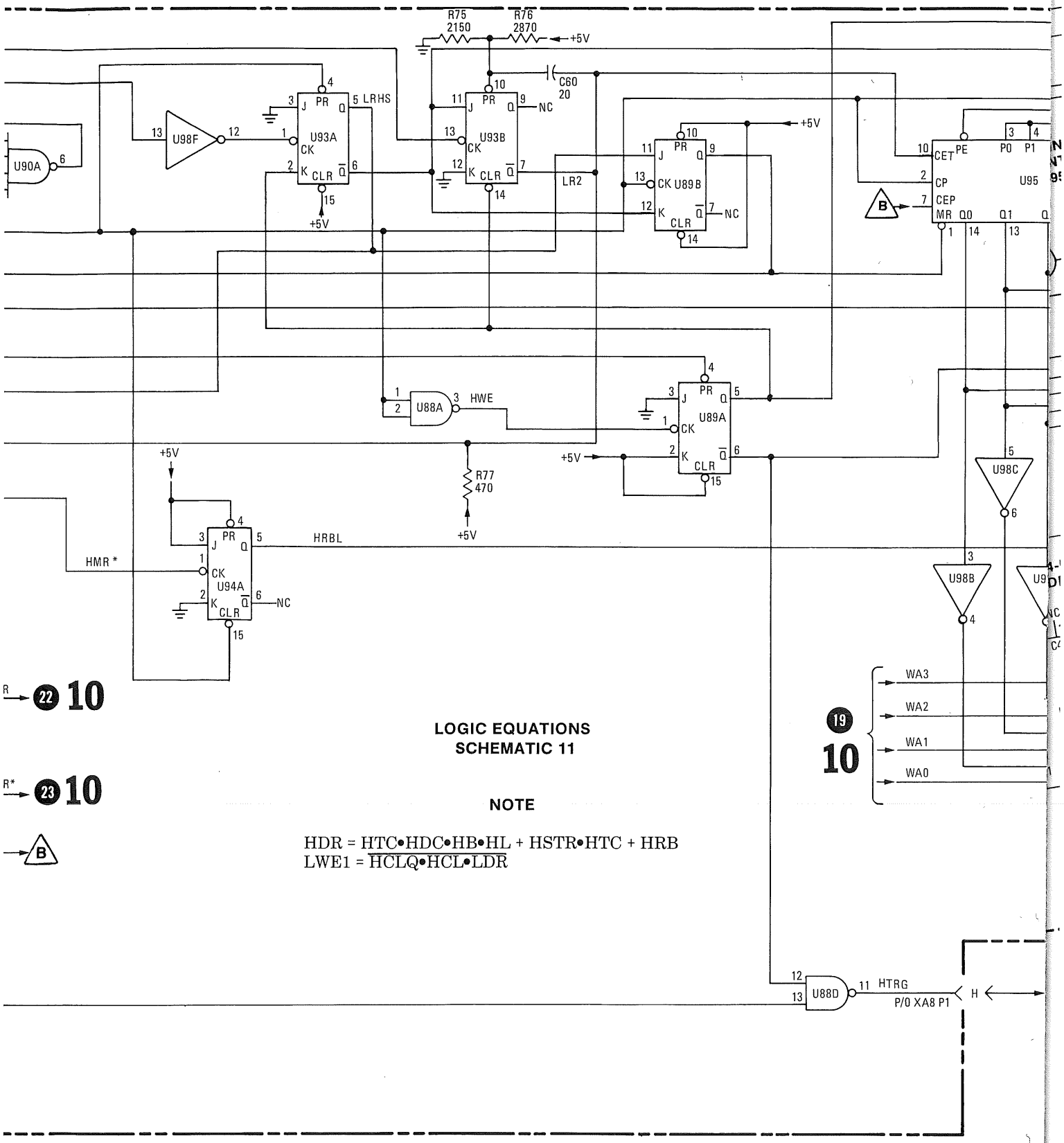


Figure 8-24. Schematic 11, Memory Index and Control

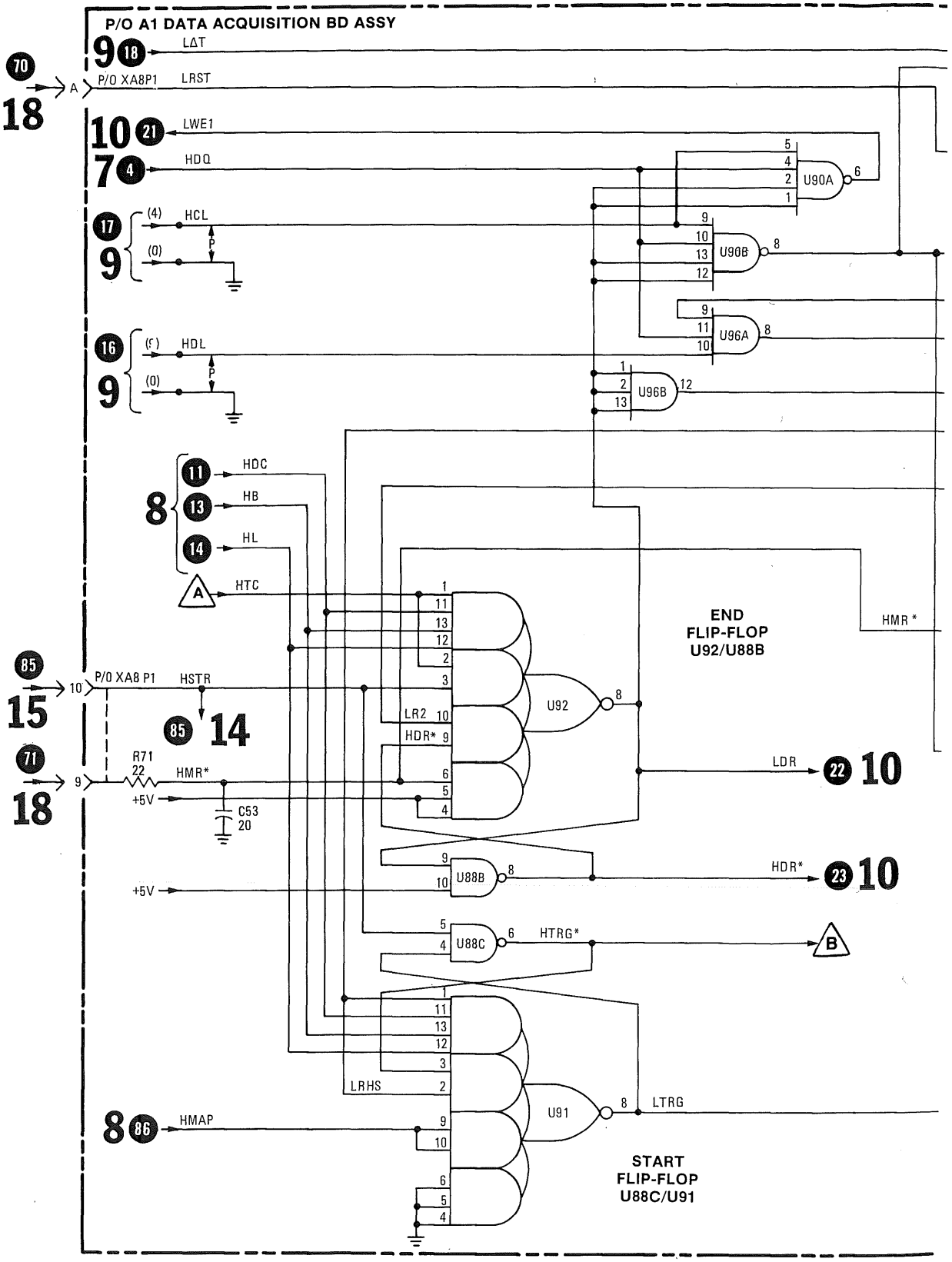


LOGIC EQUATIONS
SCHEMATIC 11

NOTE

HDR = HTC•HDC•HB•HL + HSTR•HTC + HRB

LWE1 = $\overline{\text{HCLQ•HCL•LDR}}$


P/O A1 DATA ACQUISITION BD ASSY
LΔT
P/O XA8P1
LRST
LWE1
HDQ
HCL
HDL
HDC
HB
HL
HTC
P/O XA8 P1
HSTR
R71
22
HMR*
+5V
C53
20
U90A
U90B
U96A
U96B
U92
U88B
U88C
U91
LR2
HDR*
LRHS
HMAP
HTRG*
LTRG
LDR
HDR*
HMR*
END
FLIP-FLOP
U92/U88B
START
FLIP-FLOP
U88C/U91

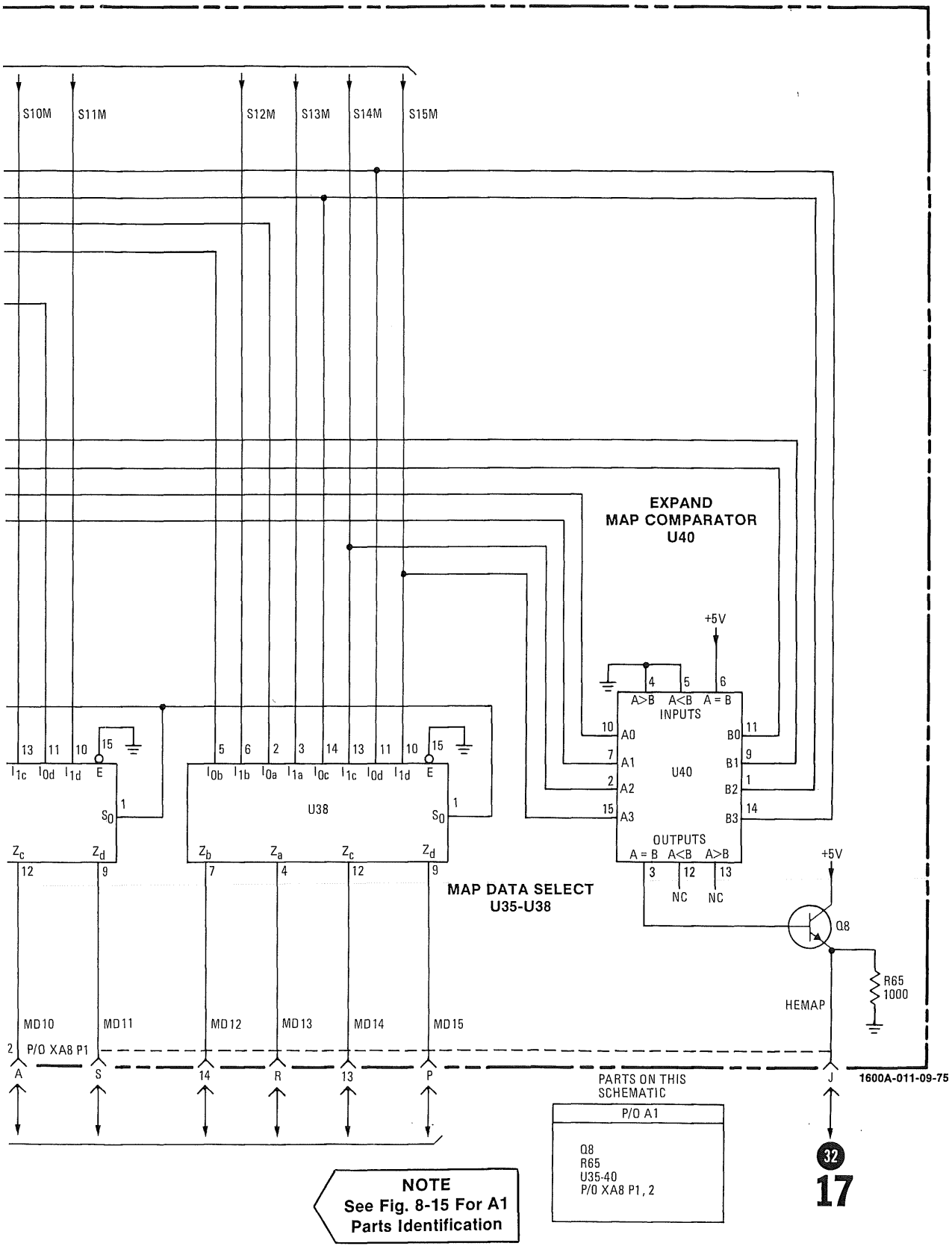
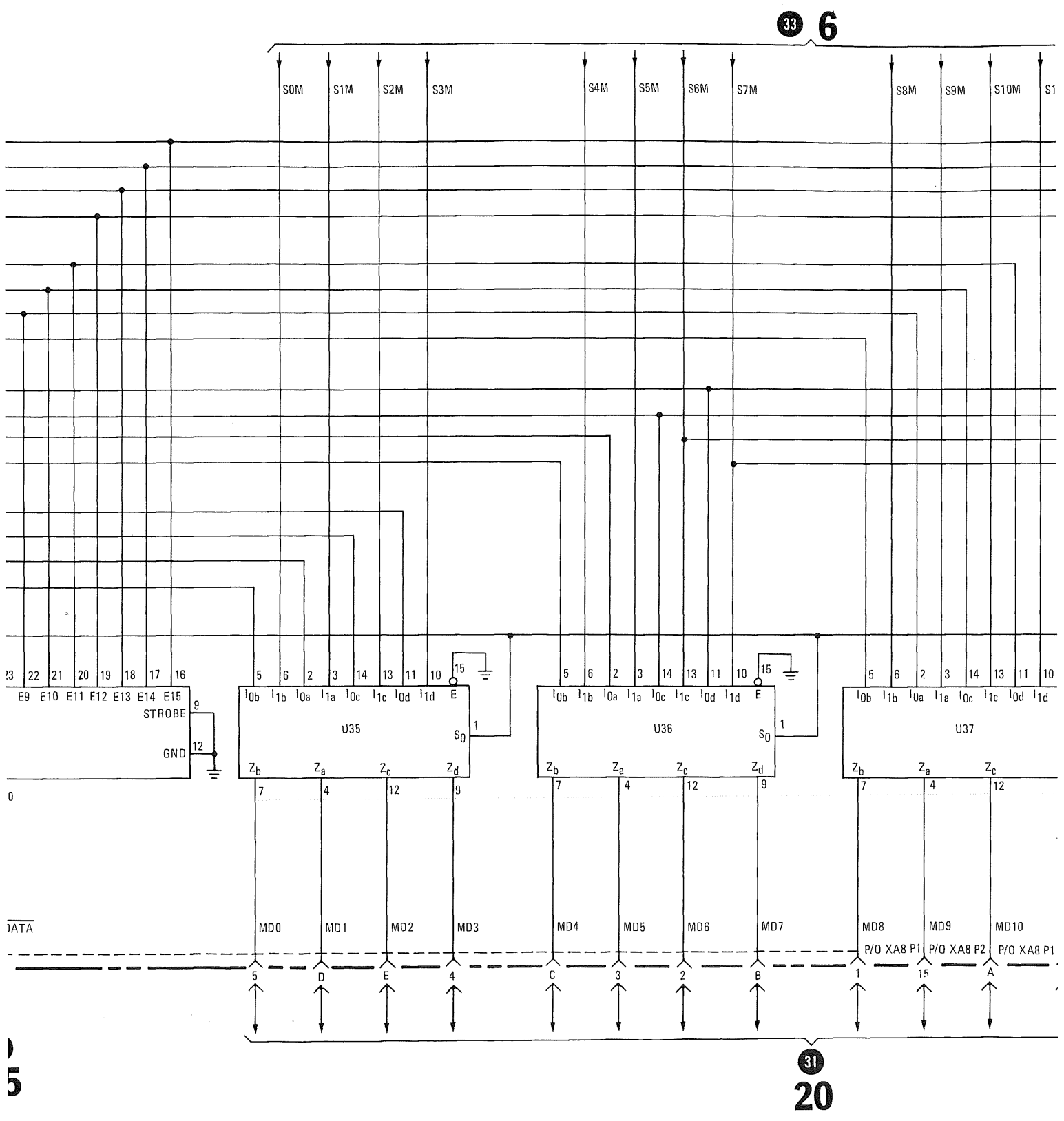
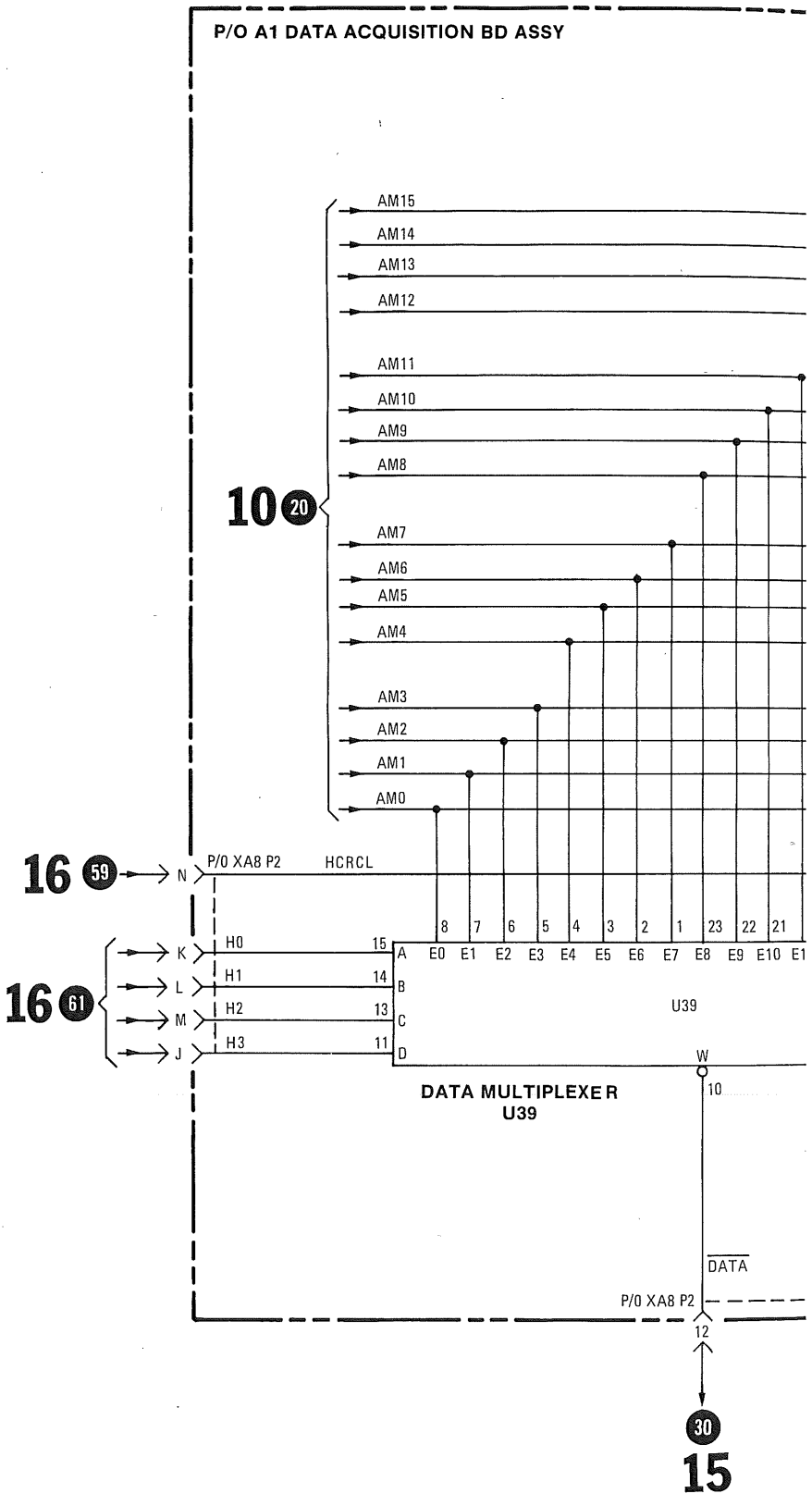


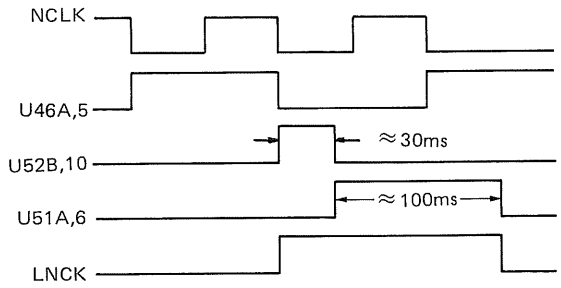
Figure 8-25.
Schematic 12, Display Data Switch


33
6
S0M
S1M
S2M
S3M
S4M
S5M
S6M
S7M
S8M
S9M
S10M
S1
E9
E10
E11
E12
E13
E14
E15
STROBE
GND
U35
U36
U37
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
P/O XA8 P1
P/O XA8 P2
P/O XA8 P1
31
20


P/O A1 DATA ACQUISITION BD ASSY
AM15
AM14
AM13
AM12
AM11
AM10
AM9
AM8
10 20
AM7
AM6
AM5
AM4
AM3
AM2
AM1
AM0
16 59
N
P/O XA8 P2
HCRCL
8 7 6 5 4 3 2 1 23 22 21
K
L
M
J
16 61
H0
H1
H2
H3
15
14
13
11
A
B
C
D
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E1
U39
W
10
DATA MULTIPLEXER
U39
DATA
P/O XA8 P2
12
30
15

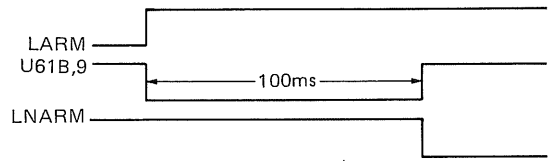
SCHEMATIC 13

NO CLOCK Timing Diagram and Truth Table



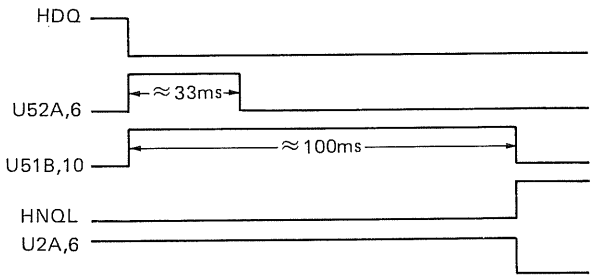
LNCK	NO CLOCK LIGHT
0	ON
1	OFF

NO ARM Timing Diagram and Truth Table



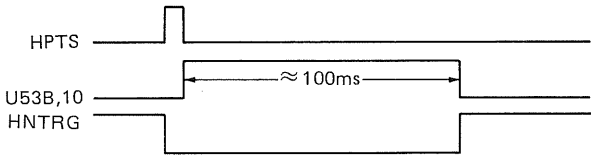
LNARM	NO ARM LIGNT
0	ON
1	OFF

NO QUAL Timing Diagram and Truth Table



LNCK	HNQL	NO QUAL LIGHT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

NO TRIG Timing Diagram and Truth Table



LNCK	HNQL	HNTRG	LNARM	NO TRIG LIGHT
0	X	X	X	OFF
1	0	X	X	OFF
1	1	1	0	OFF
1	1	1	1	ON

X = Don't Care

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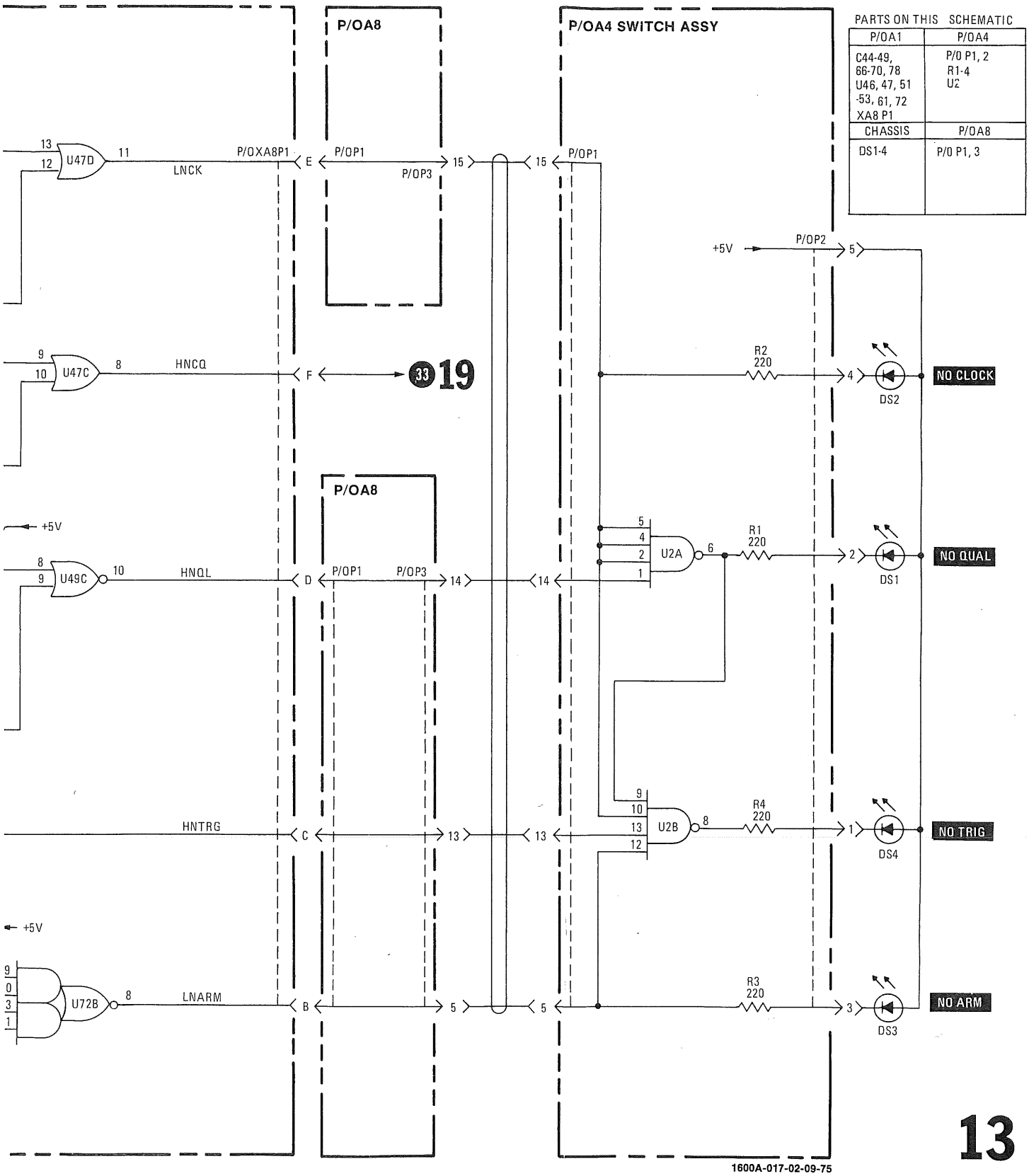
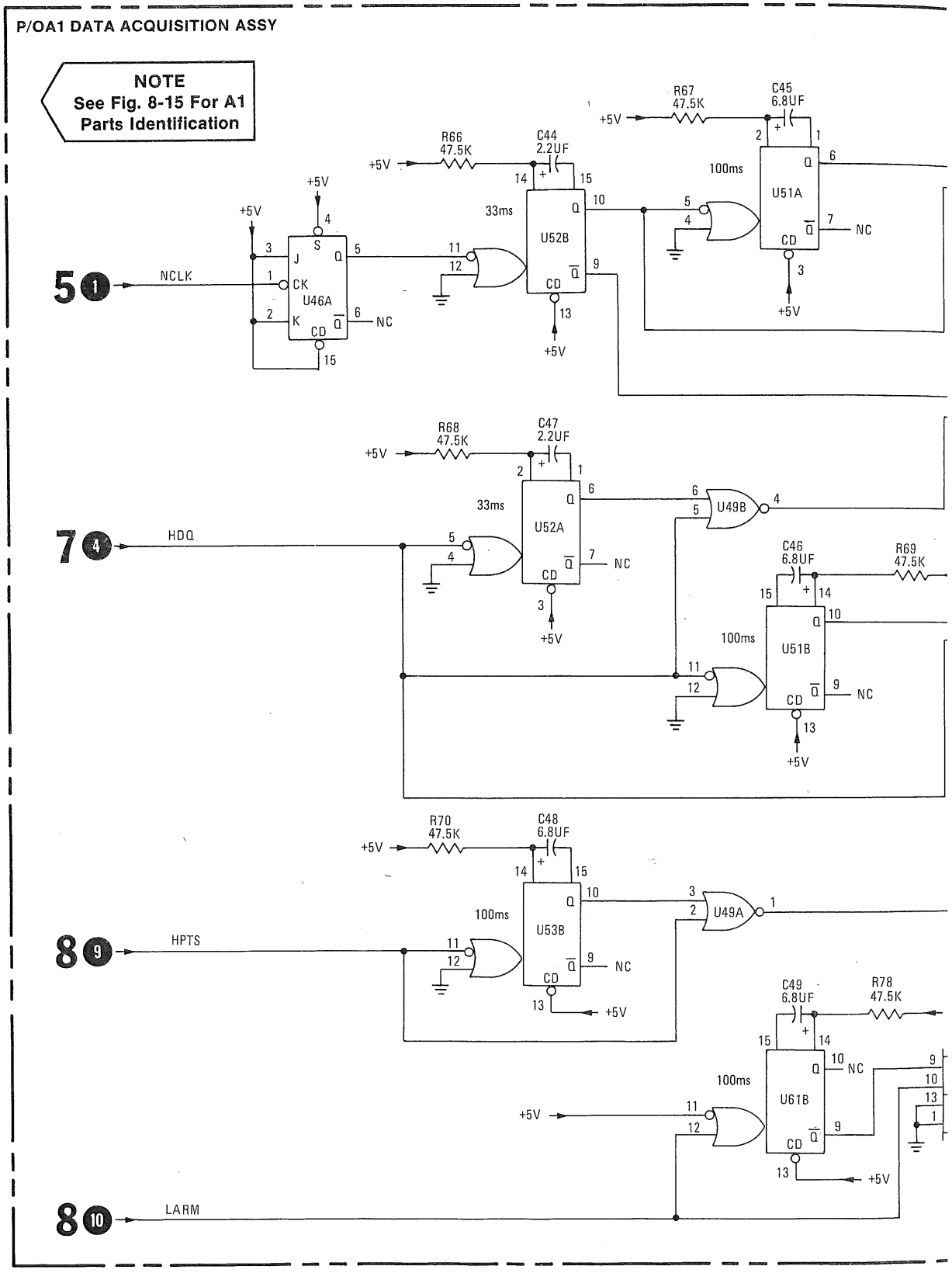
Figure 8-26. Schematic 13, Indicator Light Control (Sheet 1 of 2)



13

Figure 8-26.
Schematic 13, Indicator Light Control (Sheet 2 of 2)

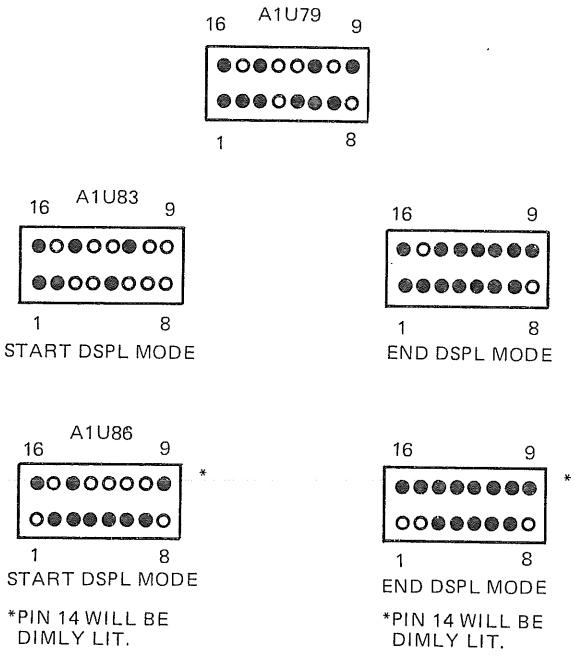

P/OA1 DATA ACQUISITION ASSY
NOTE
See Fig. 8-15 For A1
Parts Identification
5 1
NCLK
7 4
HDQ
8 9
HPTS
8 10
LARM
U46A
U52B
U51A
U52A
U49B
U51B
U53B
U49A
U61B
R66 47.5K
C44 2.2UF
R67 47.5K
C45 6.8UF
R68 47.5K
C47 2.2UF
R69 47.5K
C46 6.8UF
R70 47.5K
C48 6.8UF
R78 47.5K
C49 6.8UF
+5V
33ms
100ms
NC

SCHEMATIC 14 TROUBLESHOOTING

1. Set Model 1600A controls as follows:

SAMPLE MODE	SGL
DISPLAY MODE	START DSPL
WORD	ON
DELAY	OFF
COLUMN BLANKING	FULL CCW
LOGIC	POS
BYTE	4 BIT
DISPLAY MODE	TABLE A

2. Monitor A1U79, A1U83 and A1U86, using Model 10528A Logic Clip. The following indications will be observed when the circuit is functioning properly.



U83
Zb
1 0 1 0 1 0 1 0 1 0 1 0 1 0 X
X

Figure 8-27. Schematic 14, Word Intensity (Sheet 1 of 2)

TRIGGER WORD INTENSIFY DECODING

DELAY SETTINGS	TEN'S DECADE 2D3	2D2	2D1	2D0	UNIT'S DECADE 1D3	1D2	1D1	1D0	CARRY (A1U79, PIN 14)	MULTIPLEXER I OUTPUT CODE Za	Zc	Zd
0	1	0	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	1	0	0	0	1	1	1	1
2	1	0	0	1	0	1	1	1	1	1	1	0
3	1	0	0	1	0	1	1	0	1	1	1	0
4	1	0	0	1	0	1	0	1	1	1	0	1
5	1	0	0	1	0	1	0	0	1	1	0	1
6	1	0	0	1	0	0	1	1	1	1	0	0
7	1	0	0	1	0	0	1	0	1	1	0	0
8	1	0	0	1	0	0	0	1	1	0	1	1
9	1	0	0	1	0	0	0	0	1	0	1	1
10	1	0	0	0	1	0	0	1	1	0	1	0
11	1	0	0	0	1	0	0	0	1	0	1	0
12	1	0	0	0	0	1	1	1	1	0	0	1
13	1	0	0	0	0	1	1	0	1	0	0	1
14	1	0	0	0	0	1	0	1	1	0	0	0
15	1	0	0	0	0	1	0	0	1	0	0	0
16	1	0	0	0	0	0	1	1	0	X	X	X
17	1	0	0	0	0	0	1	0	0			
	1	0	0	0	0	0	0	1	0			
	1	0	0	0	0	0	0	0	0			
	0	X	X	X								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
X	X	X	X	X	X	X	X	X	0	X	X	X

X = DON'T CARE

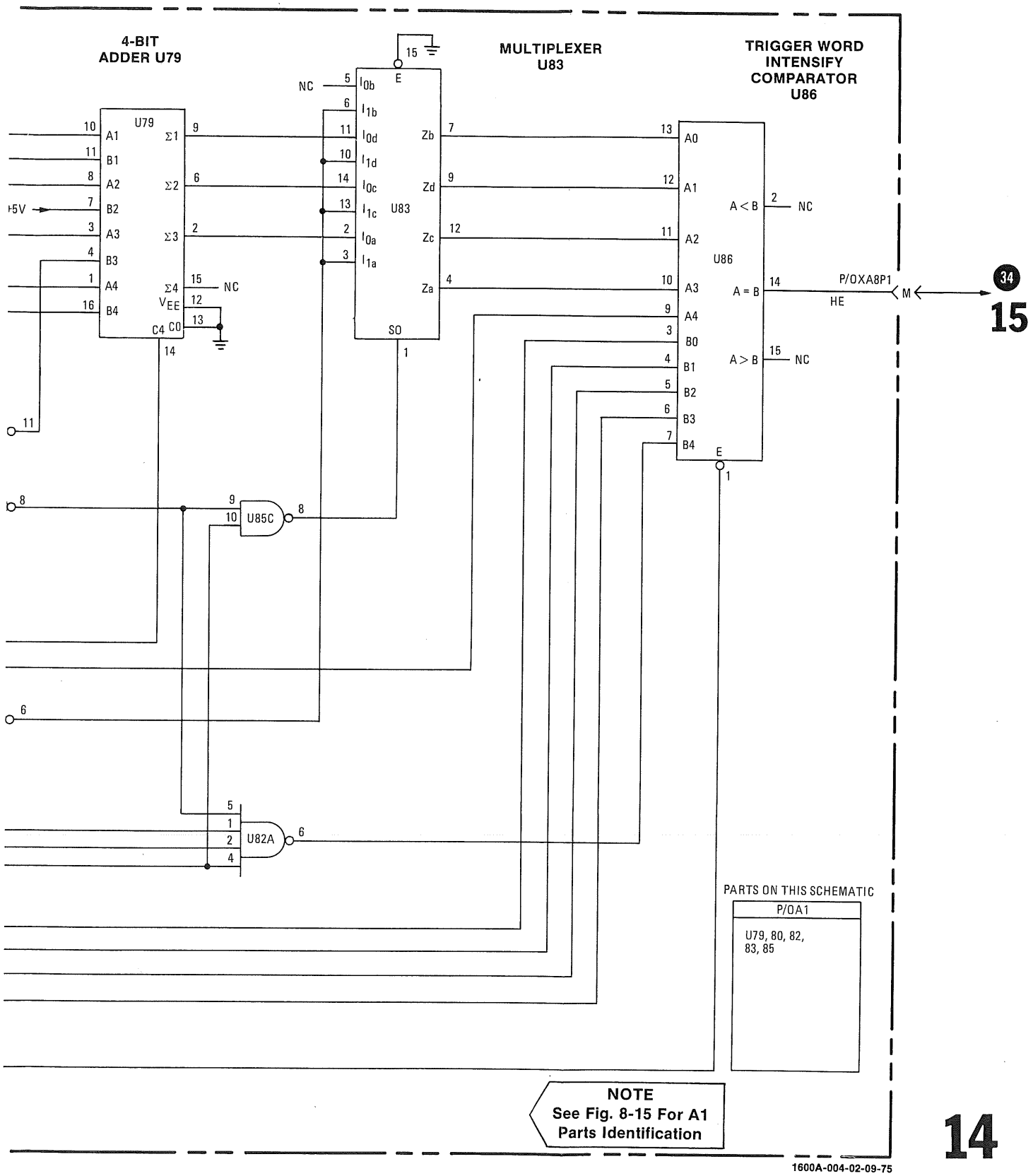
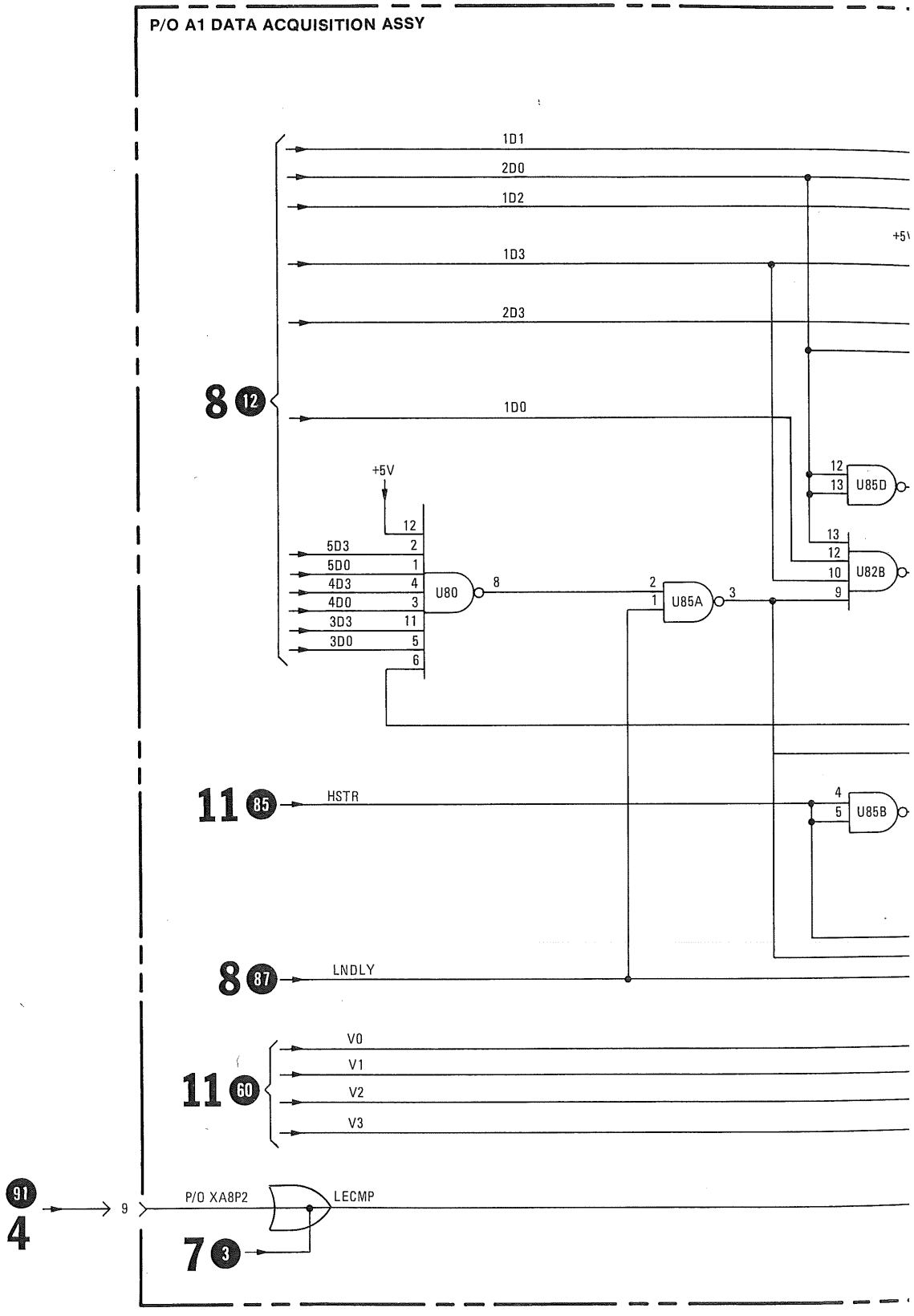


Figure 8-27.
Schematic 14, Word Intensity (Sheet 2 of 2)


P/O A1 DATA ACQUISITION ASSY
1D1
2D0
1D2
+5V
1D3
2D3
8 12
1D0
+5V
12
5D3 2
5D0 1
4D3 4
4D0 3
3D3 11
3D0 5
6
U80
8
2
1
U85A
3
12
13
U85D
13
12
10
U82B
9
11 85
HSTR
4
5
U85B
8 87
LNDLY
11 60
V0
V1
V2
V3
91
4
9
P/O XA8P2
LECMP
7 3

SCHEMATIC 15 TROUBLESHOOTING

1. Set Model 1600A controls as follows:

SAMPLE MODE	SGL
DISPLAY MODE	TABLE A & B
TRIGGER MODE	START DSPL
WORD	ON
DELAY	OFF
THUMBWHEELS	ALL 0's
COLUMN BLANKING	FULL CCW
LOGIC	POS
BYTE	4 BIT
INTENSITY	12 O'CLOCK
FOCUS	12 O'CLOCK

2. Monitor A8U32, A8U33, A8U35 with Model 10528A Logic Clip. The following indication will be observed when the circuit is functioning properly.

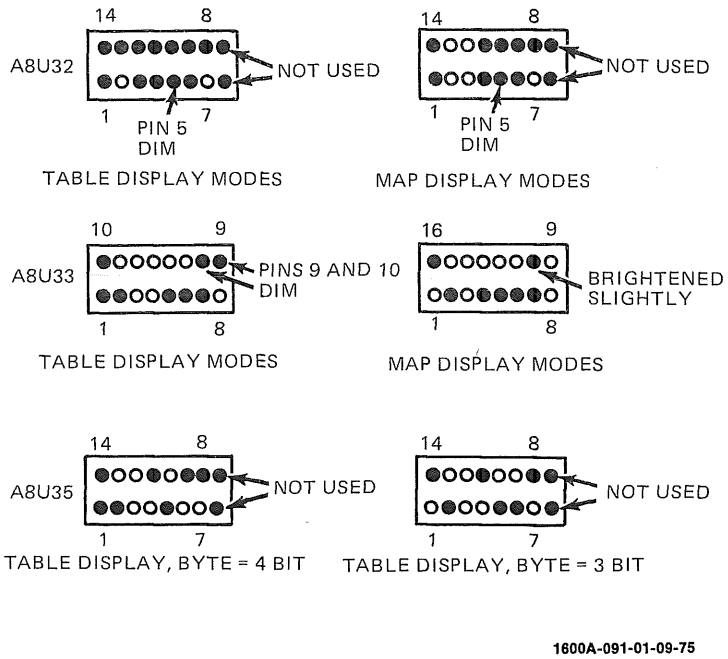


Figure 8-28. Schematic 15, Data Routing and Multiplexing (Sheet 1 of 2)

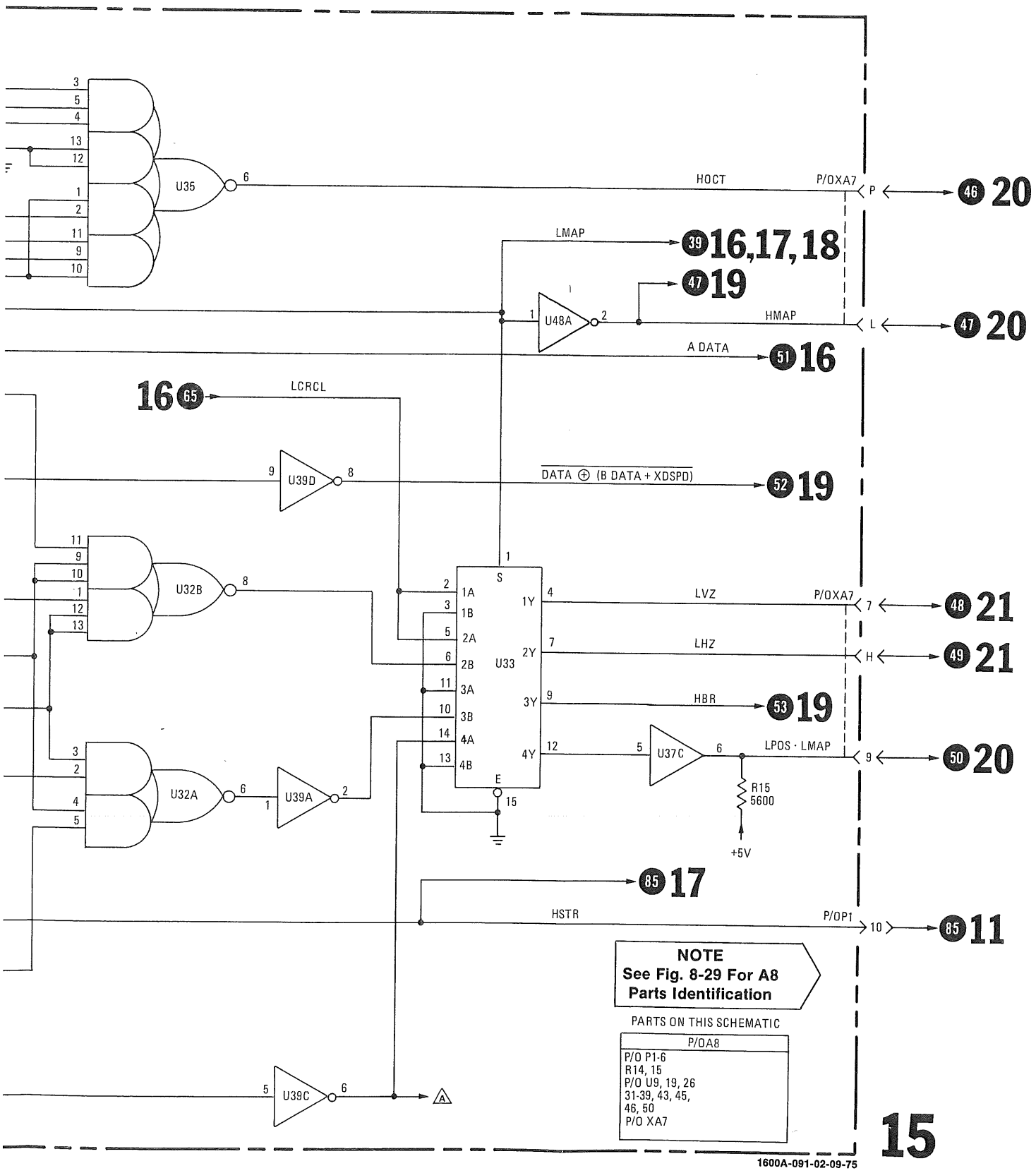
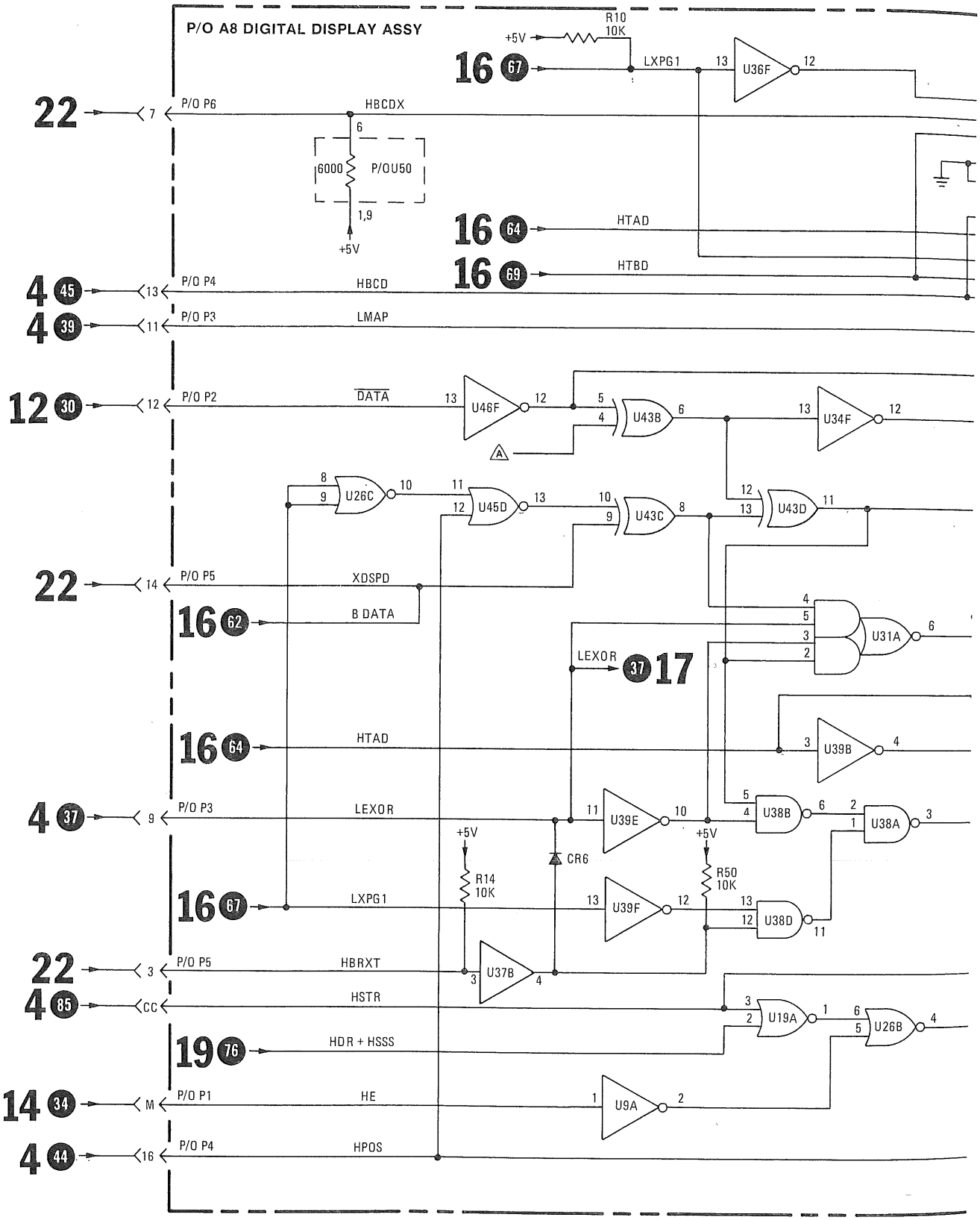
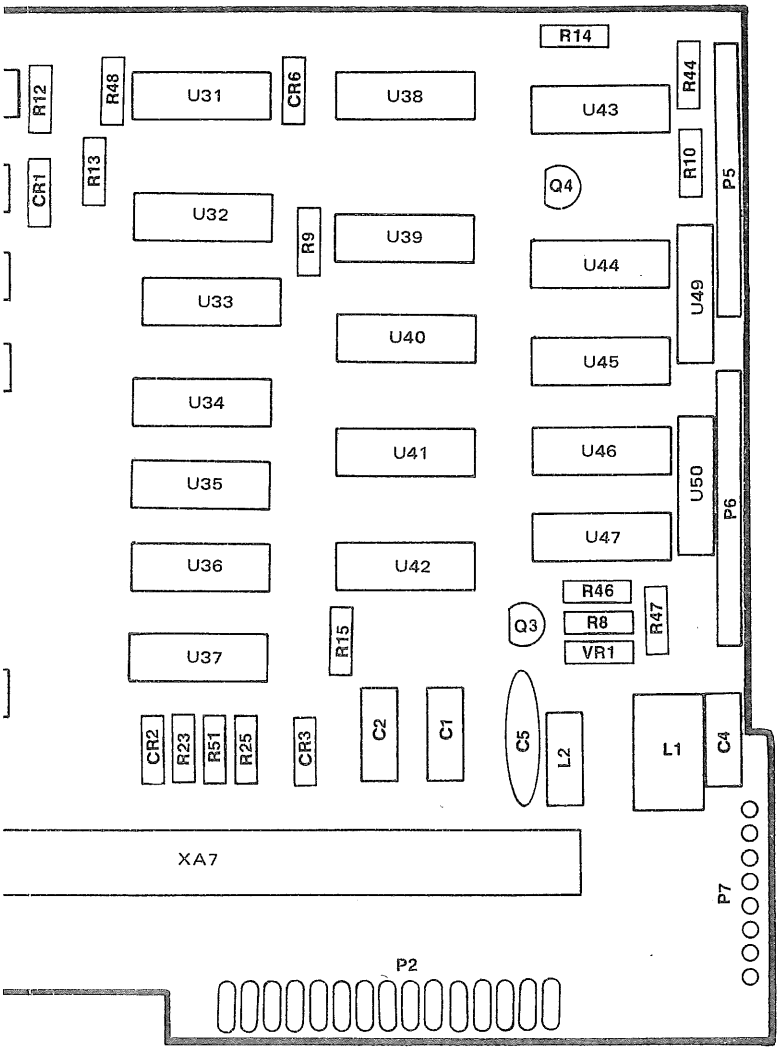


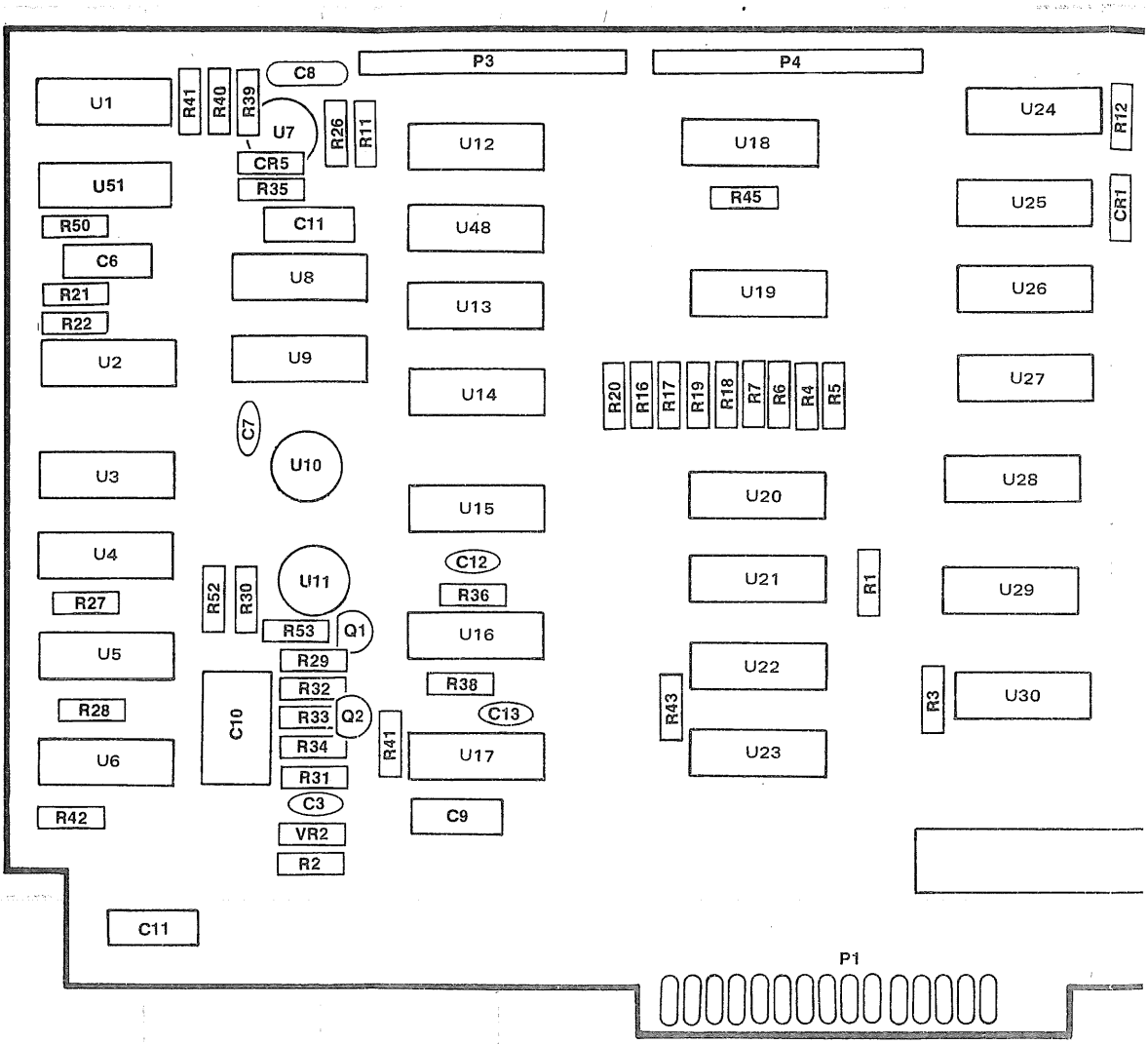
Figure 8-28.
Schematic 15, Data Routing and Multiplexing (Sheet 2 of 2)


P/O A8 DIGITAL DISPLAY ASSY
R10
10K
+5V
16 67
LXPG1
U36F
22
P/O P6
HBCDX
6000
P/OU50
1,9
+5V
16 64
HTAD
16 69
HTBD
4 45
P/O P4
HBCD
4 39
P/O P3
LMAP
12 30
P/O P2
DATA
U46F
U43B
U34F
U26C
U45D
U43C
U43D
22
P/O P5
XDSPD
16 62
B DATA
LEXOR
37 17
U31A
16 64
HTAD
U39B
4 37
P/O P3
LEXOR
U39E
U38B
U38A
CR6
R14
10K
R50
10K
16 67
LXPG1
U39F
U38D
22
P/O P5
HBRXT
U37B
4 85
HSTR
U19A
U26B
19 76
HDR + HSSS
14 34
P/O P1
HE
U9A
4 44
P/O P4
HPOS



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J-5	R38	D-4
C2	C-5	R39	C-1
C3	J-5	R40	C-1
C4	L-5	R41	C-1
C5	L-5	R42	B-5
C6	B-2	R43	E-4
C7	C-3	R44	L-1
C8	C-1	R45	F-2
C9	D-5	R46	K-4
C10	C-5	R47	K-4
C11	C-2	R48	H-1
C12	C-4	R49	L-1
C13	E-4	R50	B-2
C14	L-5	R51	I-5
CR1	H-2	U1	B-1
CR2	I-5	U2	B-2
CR3	I-5	U3	B-3
CR5	C-1	U4	B-4
CR6	I-1	U5	B-4
L1	K-5	U6	B-5
L2	K-5	U7	C-1
P1	F-6	U8	C-2
P2	F-6	U9	C-2
P3	D-1	U10	C-3
P4	F-1	U11	C-4
P5	L-2	U12	D-1
P6	L-3	U13	D-2
P7	L-6	U14	D-3
Q1	D-4	U15	D-3
Q2	D-4	U16	D-4
Q3	K-4	U17	D-5
Q4	K-2	U18	F-1
R1	G-4	U19	F-2
R2	C-5	U20	F-3
R3	G-4	U21	F-4
R4	F-3	U22	F-4
R5	F-3	U23	F-5
R6	F-3	U24	H-1
R7	F-3	U25	G-2
R8	K-4	U26	G-2
R9	I-2	U27	G-3
R10	L-2	U28	G-3
R11	D-1	U29	G-4
R12	H-1	U30	G-4
R13	H-2	U31	I-1
R14	K-1	U32	I-2
R15	J-3	U33	I-2
R16	E-3	U34	I-3
R17	E-3	U35	I-3
R18	F-3	U36	I-4
R19	F-3	U37	I-4
R20	E-3	U38	J-1
R21	B-2	U39	J-2
R22	B-2	U40	J-3
R23	I-5	U41	J-3
R25	I-5	U42	J-2
R26	D-1	U43	K-1
R27	B-4	U44	K-2
R28	B-4	U45	K-3
R29	C-4	U46	K-3
R30	C-4	U47	K-4
R31	C-5	U48	D-1
R32	C-4	U49	L-2
R33	C-4	U50	L-3
R34	C-5	U51	B-2
R35	C-2	VR1	K-4
R36	D-4	VR2	C-5
R37	C-5	XA7	I-5

Figure 8-29. Parts Identification, Board Assembly A8


P3
P4
U1
R41
R40
R39
C8
U7
R26
R11
U12
U18
U24
R12
CR5
R35
U51
R45
U25
CR1
R50
C11
U48
C6
U8
U19
U26
R21
U13
R22
U2
U9
U14
U27
R20
R16
R17
R19
R18
R7
R6
R4
R5
C7
U10
U3
U15
U20
U28
U4
C12
U11
U21
R1
U29
R52
R30
R36
R27
R53
Q1
U16
U5
R29
U22
U30
R32
R38
R43
R3
R28
C10
R33
Q2
C13
R34
R41
U17
U23
U6
R31
C3
C9
R42
VR2
R2
C11
P1

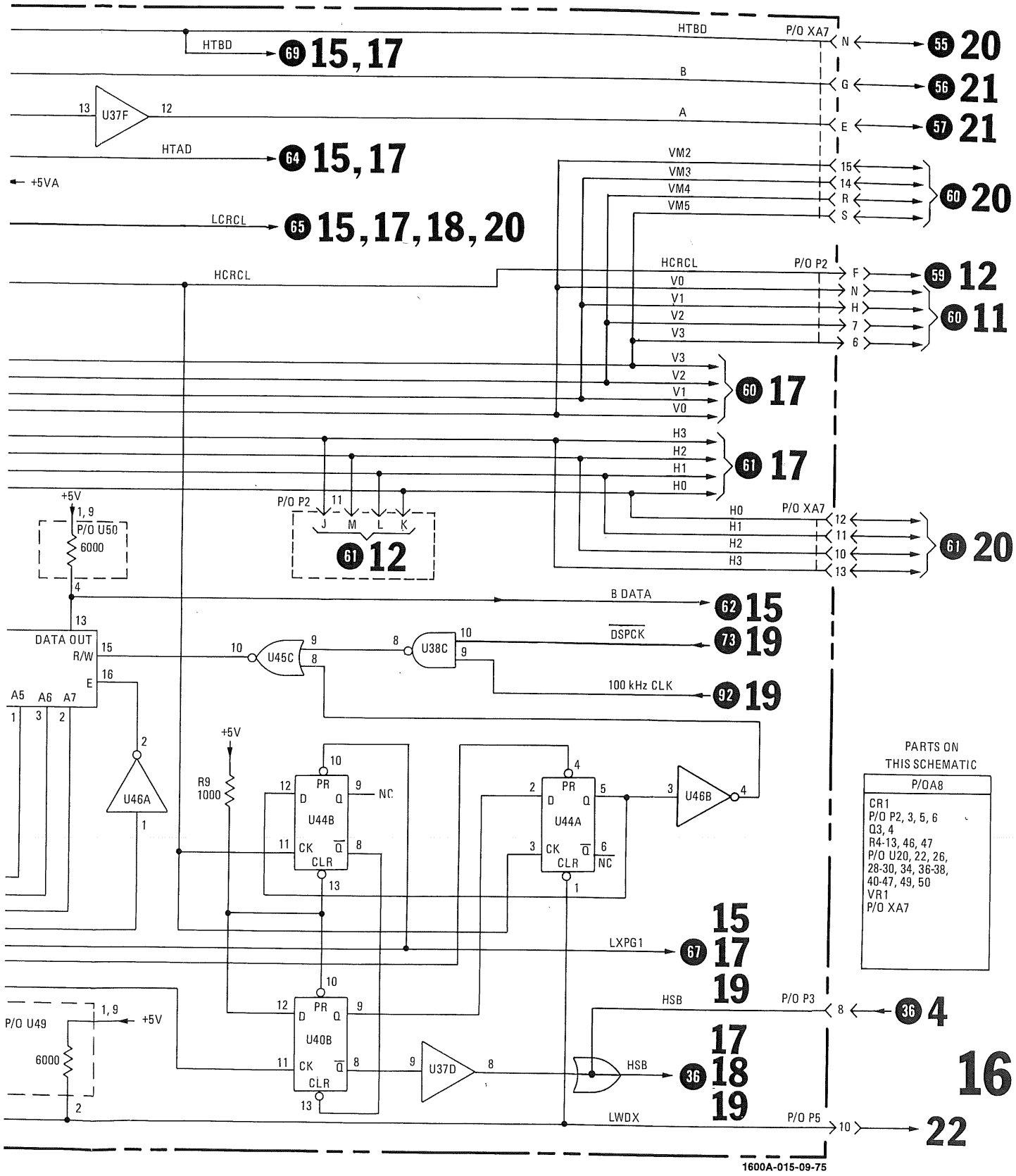
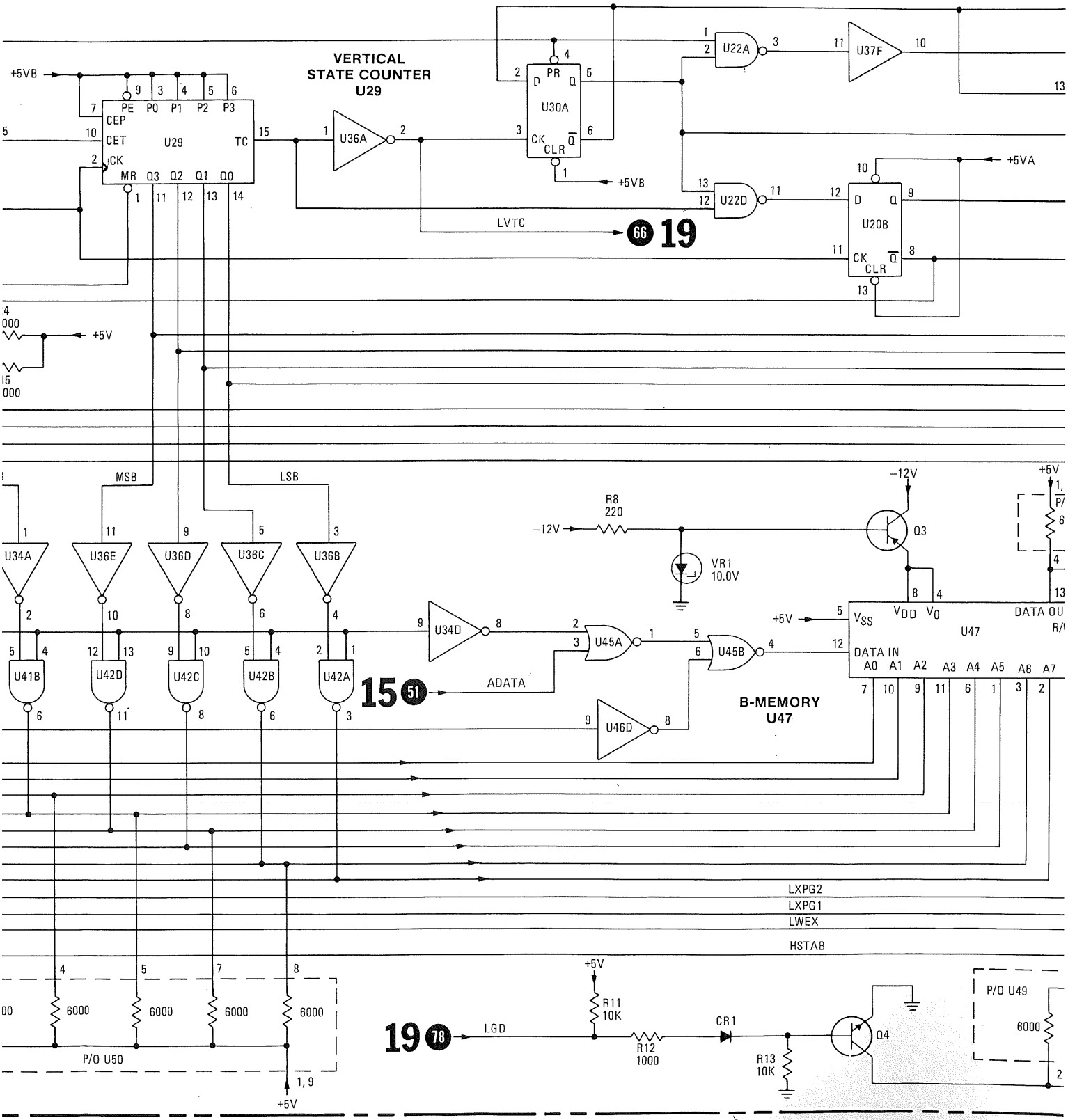
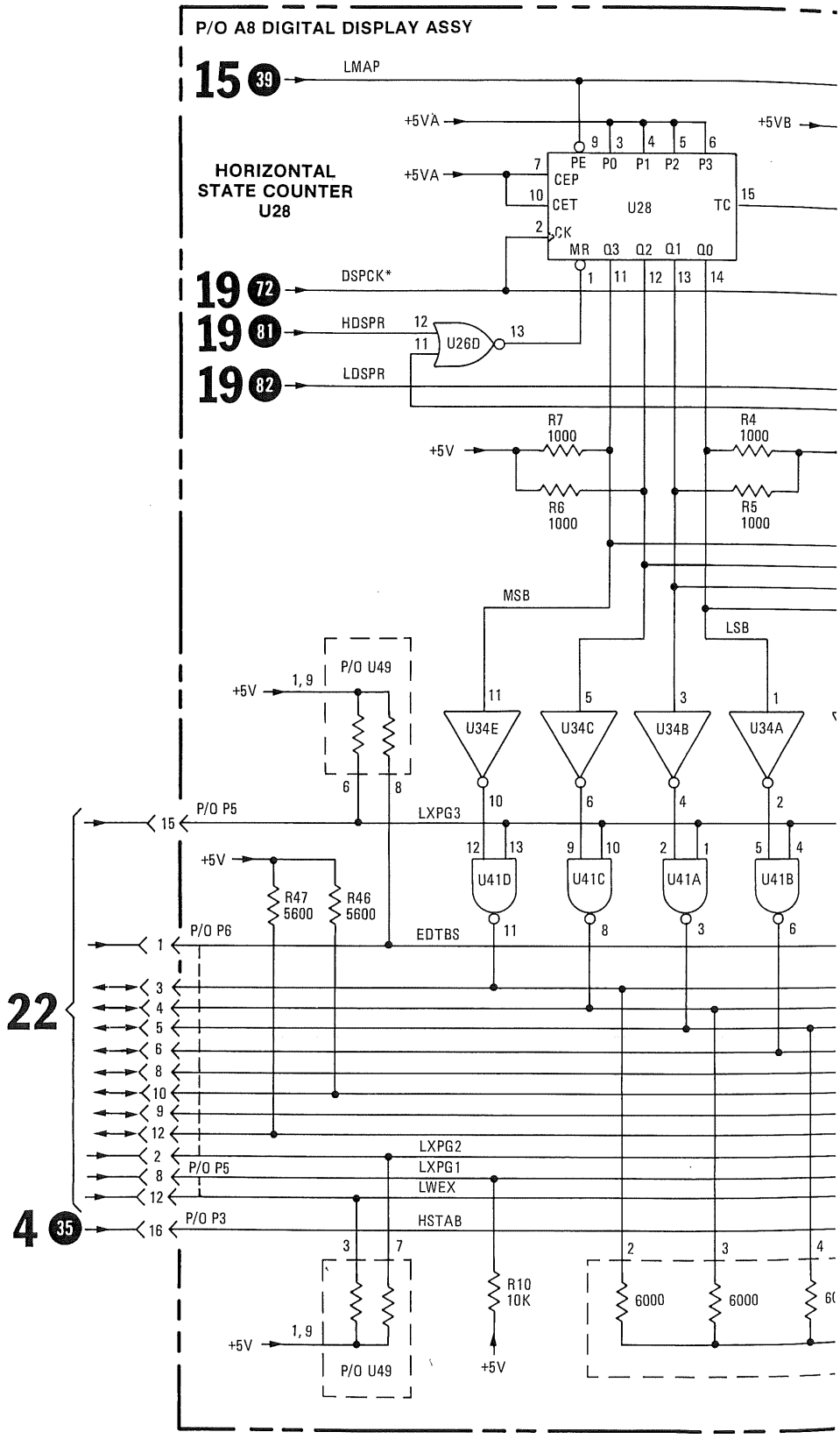


Figure 8-30.
Schematic 16, Display Counters and B-memory


VERTICAL
STATE COUNTER
U29
+5VB
PE P0 P1 P2 P3
CEP
CET
CK
MR Q3 Q2 Q1 Q0
U29
TC
U36A
U30A
PR
CK
CLR
U22A
U37F
U22D
U20B
+5VA
LVTC
66 19
+5V
MSB
LSB
U34A
U36E
U36D
U36C
U36B
U41B
U42D
U42C
U42B
U42A
U34D
U45A
U45B
U46D
15 51
ADATA
R8
220
−12V
VR1
10.0V
Q3
B-MEMORY
U47
DATA IN
A0 A1 A2 A3 A4 A5 A6 A7
DATA OU
LXPG2
LXPG1
LWEX
HSTAB
6000
P/O U50
1, 9
19 78
LGD
R11
10K
R12
1000
CR1
R13
10K
Q4
P/O U49


P/O A8 DIGITAL DISPLAY ASSY
HORIZONTAL STATE COUNTER U28
LMAP
+5VA
+5VB
PE P0 P1 P2 P3
CEP
CET
U28
TC
CK
MR Q3 Q2 Q1 Q0
DSPCK*
HDSPR
U26D
LDSPR
R7 1000
R4 1000
R6 1000
R5 1000
MSB
LSB
P/O U49
U34E
U34C
U34B
U34A
P/O P5
LXPG3
U41D
U41C
U41A
U41B
R47 5600
R46 5600
P/O P6
EDTBS
LXPG2
LXPG1
LWEX
HSTAB
P/O P3
R10 10K
6000
6000

SCHEMATIC 17

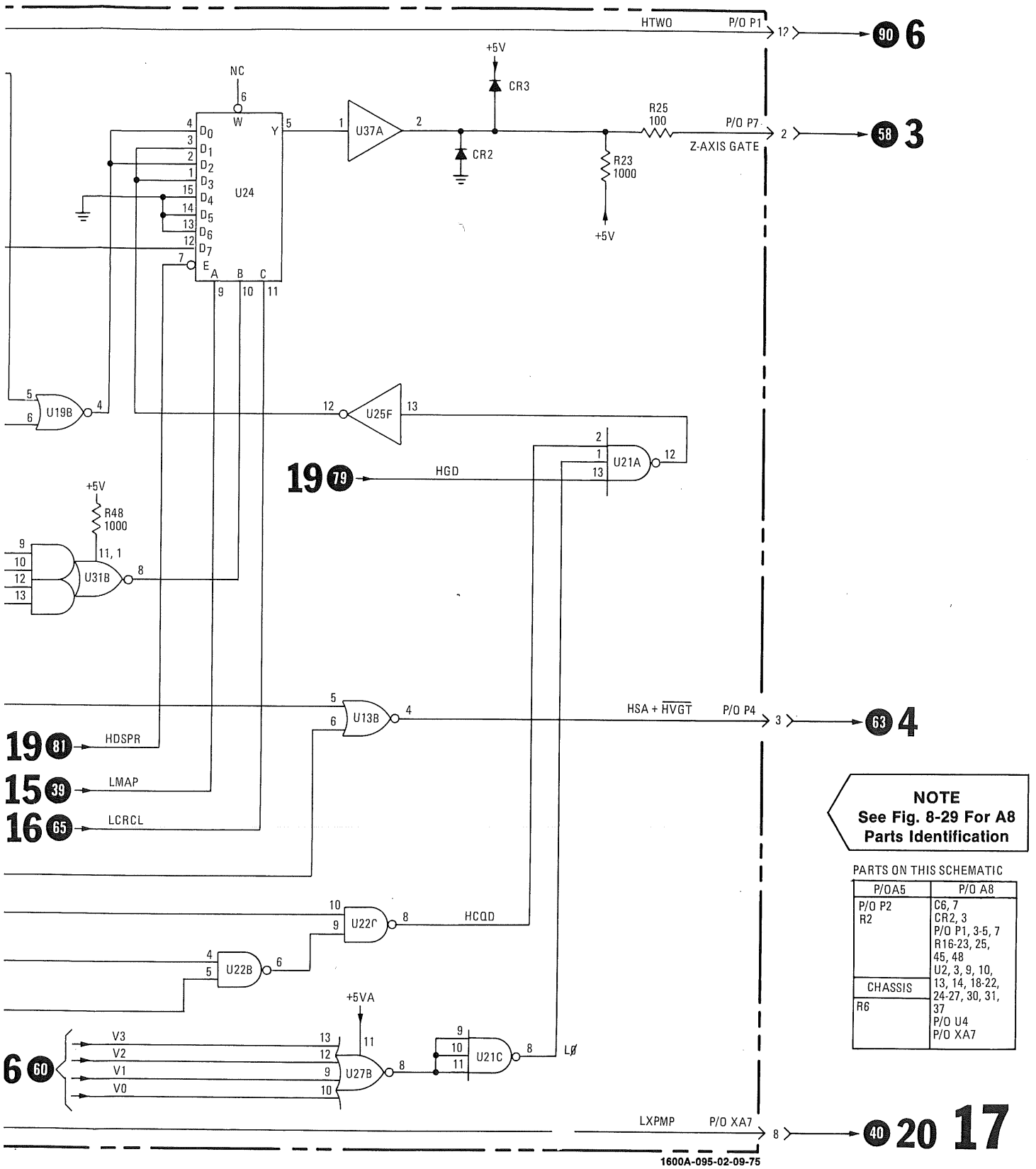
BLANKING TRUTH TABLE

A8U18 SELECT LINES			A8U24 SELECT LINES			A8U18 ENABLE (DSPCK*)	A8U24 ENABLE (HDSPR)	A8U24 Y OUTPUT (Blanking signal, TRUE in 0 state)
HTBD	LEXOR	LXPG1	LMAP	$\overline{HSA \bullet HTAD + HSB \bullet HTBD}$	LCRCL			
X	X	X	X	X	X	X	1	0
X	X	X	0	0	0	X	0	HTWO + $\overline{DSPCK*}$
X	X	X	0	0	1	X	0	HGD•HCQD•LØ
X	X	X	0	1	0	X	0	HTWO + $\overline{DSPCK*}$
X	X	X	0	1	1	X	0	HGD•HCQD•LØ
X	X	X	1	0	0	X	0	0
X	X	X	1	0	1	X	0	0
X	X	X	1	1	0	X	0	0
X	X	X	1	1	1	1	0	0
0	0	0	1	1	1	0	0	A8U14, PIN 6
0	0	1	1	1	1	0	0	A8U14, PIN 6
0	1	0	1	1	1	0	0	A8U14, PIN 6
0	1	1	1	1	1	0	0	A8U14, PIN 6
1	0	0	1	1	1	0	0	LXBLK + A8U14, PIN 6
1	0	1	1	1	1	0	0	A8U14, PIN 6
1	1	0	1	1	1	0	0	$\underline{LXBLK}$
1	1	1	1	1	1	0	0	$\overline{HCBLK}$

1. X = Don't Care
2. A8U14, PIN 6 = 0 when:
   a. HCBLK = 1
   b. HUGT•$\underline{LSSS}$ = 1
   c. HSTR•$\overline{HTRG}$ = 1
   d. LGD = 1 and the qualified clock rate is greater than ≈ 30 Hz.

1600A-095-01-09-75

Figure 8-31. Schematic 17, Blanking Control (Sheet 1 of 2)

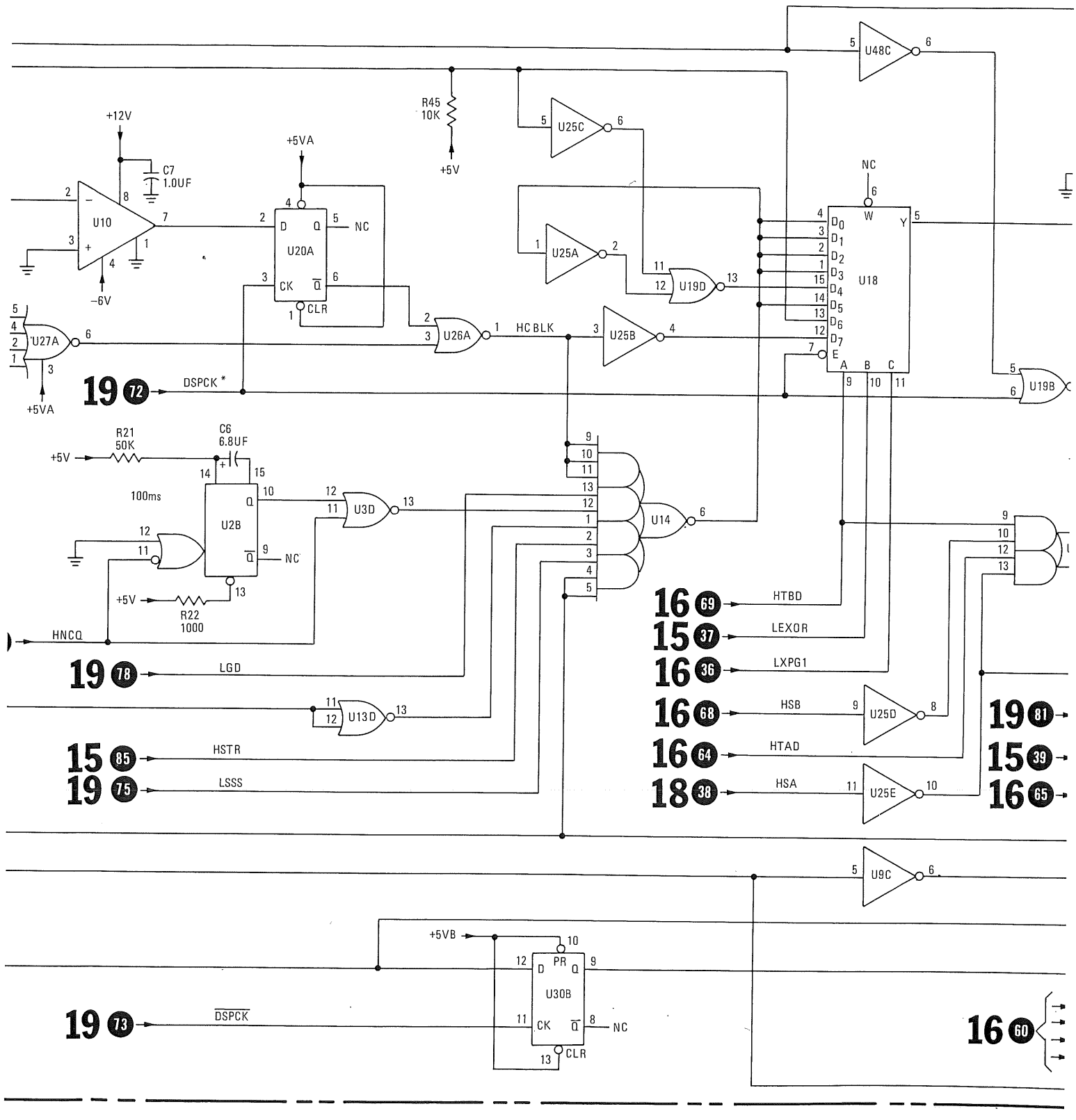


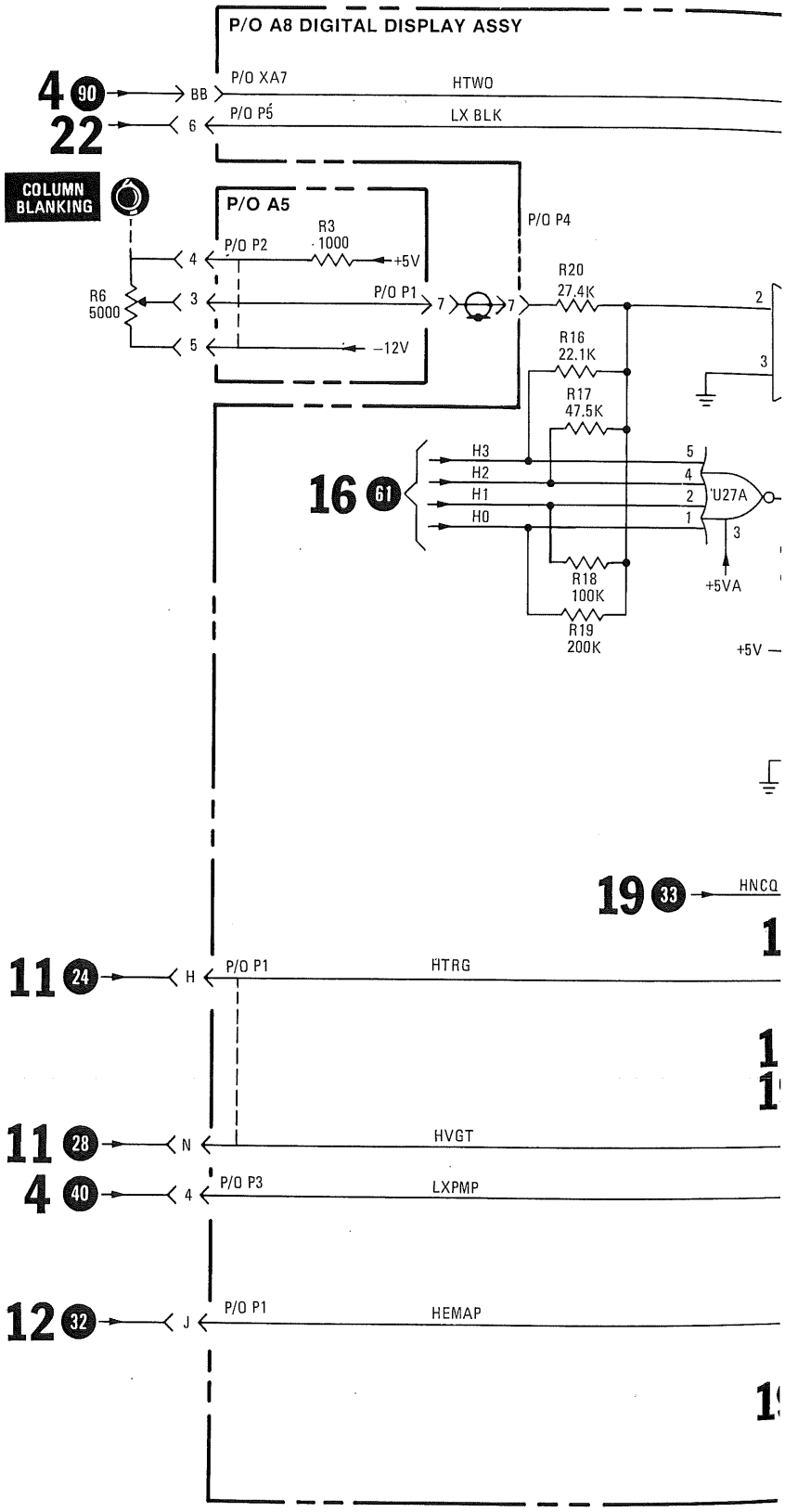
NOTE
See Fig. 8-29 For A8 Parts Identification

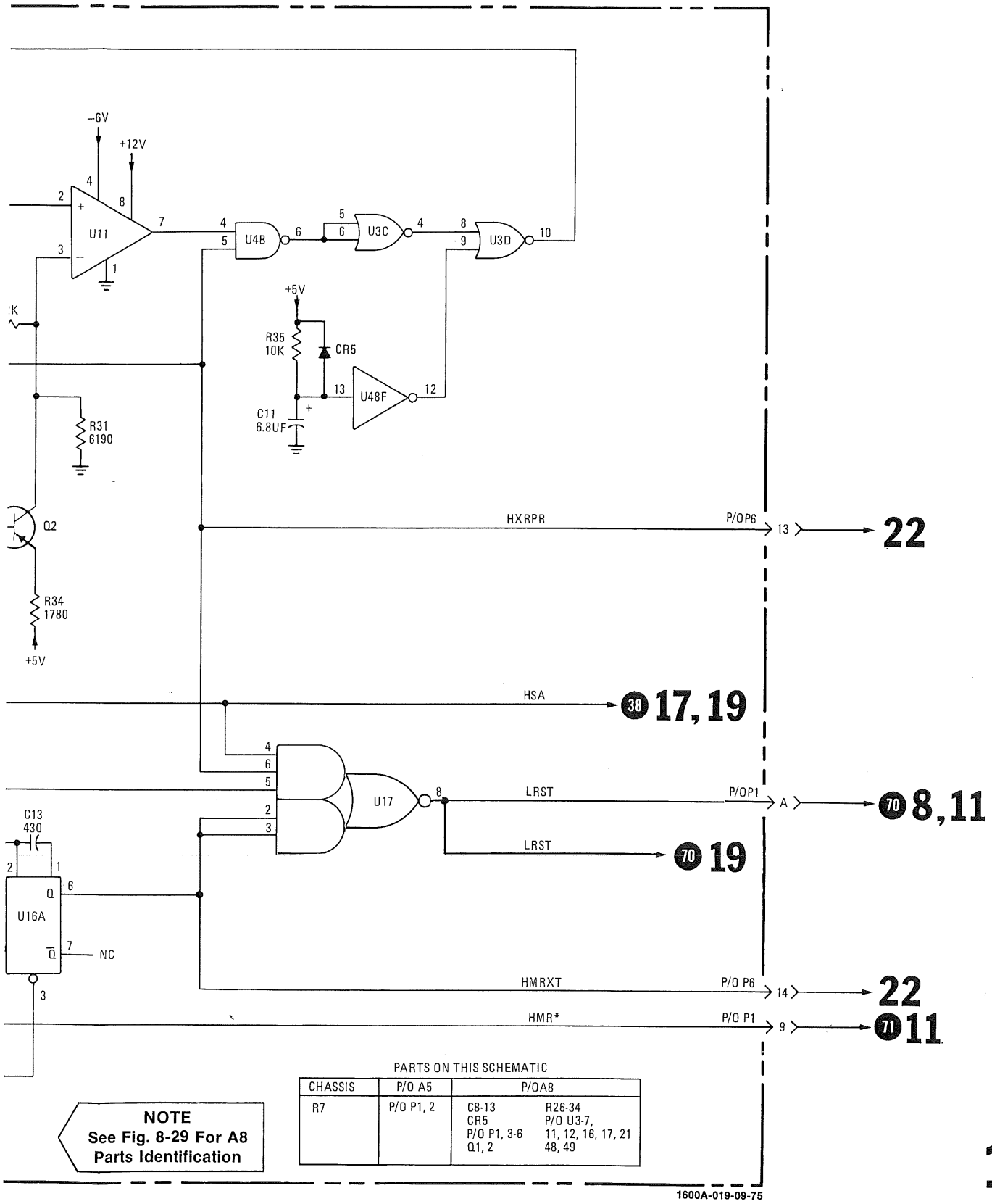
PARTS ON THIS SCHEMATIC

P/OA5	P/O A8
P/O P2 R2	C6, 7 CR2, 3 P/O P1, 3-5, 7 R16-23, 25, 45, 48 U2, 3, 9, 10, 13, 14, 18-22, 24-27, 30, 31, 37 P/O U4 P/O XA7
CHASSIS	
R6	

Figure 8-31.
Schematic 17, Blanking Control (Sheet 2 of 2)


U48C
R45
10K
+5V
U25C
+12V
C7
1.0UF
+5VA
U10
U20A
NC
U25A
U19D
U18
NC
W
Y
D0
D1
D2
D3
D4
D5
D6
D7
E
A
B
C
-6V
U27A
U26A
HC BLK
U25B
+5VA
19 72
DSPCK *
U19B
R21
50K
C6
6.8UF
+5V
100ms
U2B
U3D
U14
HTBD
16 69
LEXOR
15 37
LXPG1
16 36
HSB
16 68
U25D
19 81
HTAD
16 64
15 39
HSA
18 38
U25E
16 65
R22
1000
HNCQ
19 18
LGD
U13D
15 85
HSTR
19 75
LSSS
U9C
+5VB
U30B
19 73
DSPCK
16 60
CK
CLR
PR


P/O A8 DIGITAL DISPLAY ASSY
4 90
22
P/O XA7
BB
HTWO
P/O P5
6
LX BLK
COLUMN BLANKING
P/O A5
P/O P4
R3
1000
P/O P2
4
+5V
R6
5000
3
P/O P1
7
7
R20
27.4K
2
5
–12V
R16
22.1K
3
R17
47.5K
16 61
H3
H2
H1
H0
5
4
2
1
U27A
3
R18
100K
+5VA
R19
200K
+5V
19 33
HNCQ
11 24
H
P/O P1
HTRG
11 28
N
HVGT
4 40
4
P/O P3
LXPMP
12 32
J
P/O P1
HEMAP

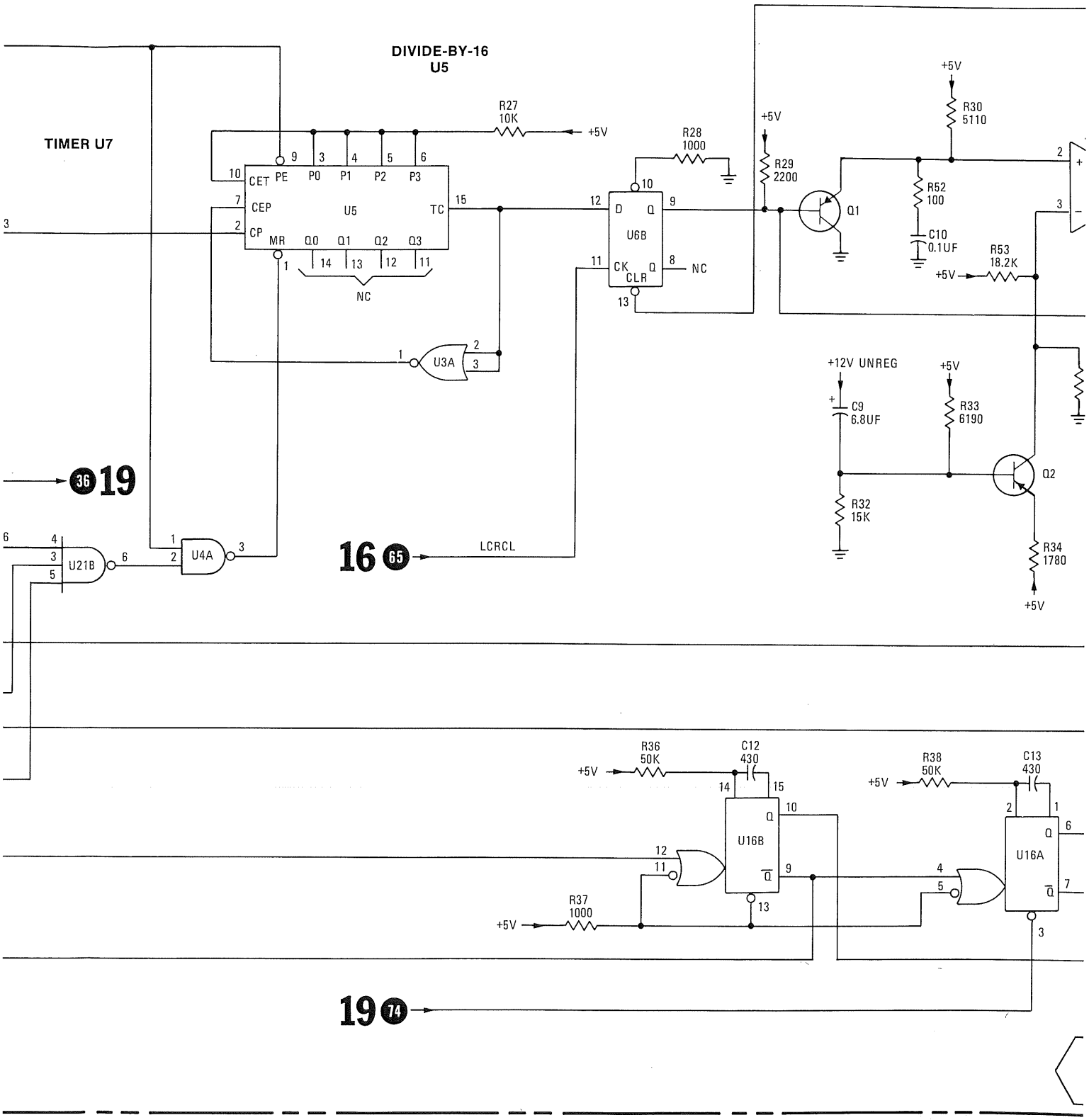


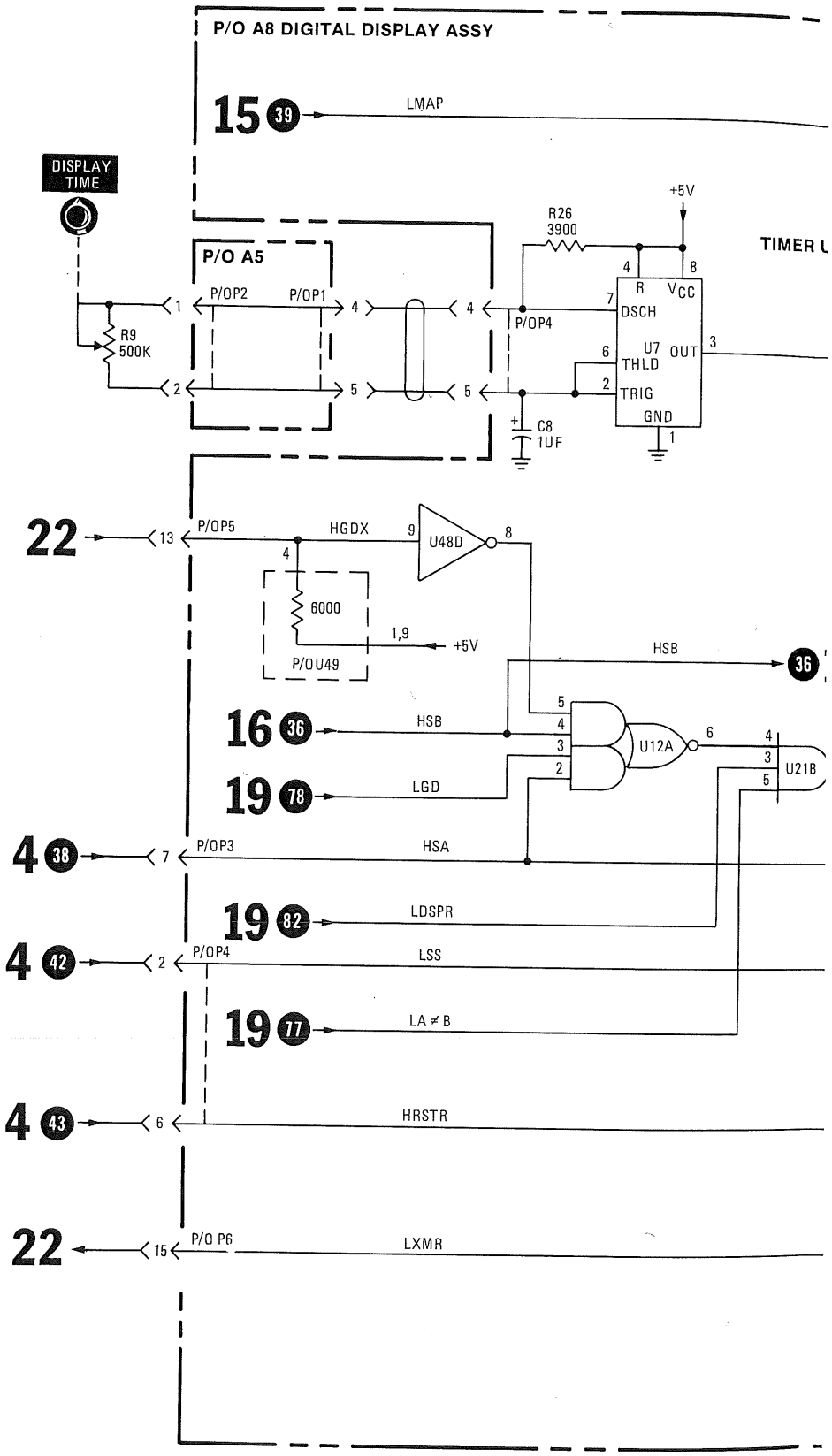
PARTS ON THIS SCHEMATIC

CHASSIS	P/O A5	P/OA8	
R7	P/O P1, 2	C8-13 CR5 P/O P1, 3-6 Q1, 2	R26-34 P/O U3-7, 11, 12, 16, 17, 21 48, 49

NOTE
See Fig. 8-29 For A8 Parts Identification

Figure 8-32.
Schematic 18, Data Acquisition Reset Circuitry


DIVIDE-BY-16
U5
TIMER U7
R27
10K
+5V
R28
1000
R29
2200
R30
5110
R52
100
C10
0.1UF
R53
18.2K
Q1
U5
CET
PE
P0
P1
P2
P3
CEP
CP
MR
Q0
Q1
Q2
Q3
TC
NC
U6B
D
Q
CK
CLR
U3A
U4A
U21B
LCRCL
+12V UNREG
C9
6.8UF
R33
6190
Q2
R32
15K
R34
1780
19
65
19
74
R36
50K
C12
430
R38
50K
C13
430
U16B
U16A
R37
1000


P/O A8 DIGITAL DISPLAY ASSY
15 39
LMAP
DISPLAY TIME
P/O A5
R9 500K
P/OP2
P/OP1
R26 3900
+5V
P/OP4
R
Vcc
DSCH
U7
THLD
OUT
TRIG
GND
C8 1UF
TIMER
22
P/OP5
HGDX
U48D
6000
1,9
+5V
P/OU49
HSB
36
16 36
HSB
19 78
LGD
U12A
U21B
4 38
P/OP3
HSA
19 82
LDSPR
4 42
P/OP4
LSS
19 77
LA ≠ B
4 43
HRSTR
22
P/O P6
LXMR

SCHEMATIC 19
WAVEFORM MEASUREMENT CONDITIONS

Set Model 1600A controls as follows:

SAMPLE MODE	SGL
DISPLAY MODE	TABLE A & B
TRIGGER MODE	START DSPL
WORD	ON
DELAY	OFF
THUMBWHEELS	ALL 0's
COLUMN BLANKING	FULL CCW
LOGIC	POS
BYTE	4 BIT
INTENSITY	12 O'CLOCK
FOCUS	12 O'CLOCK

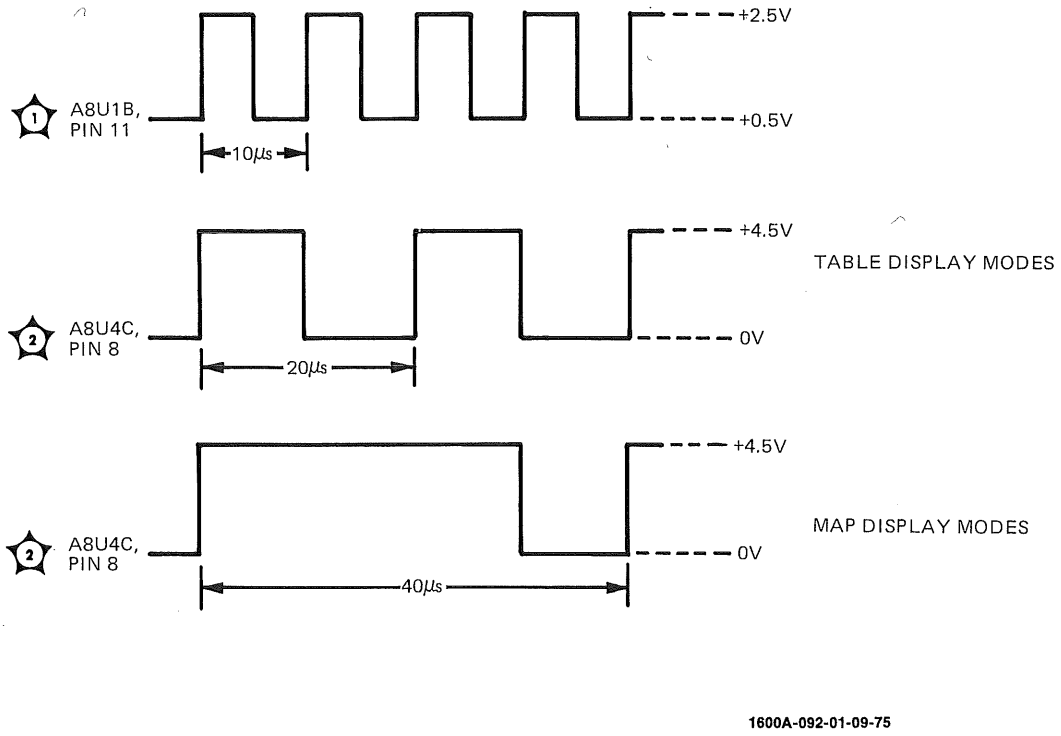


Figure 8-33.
Schematic 19, Display Clock Generator and Display Reset (Sheet 1 of 2)

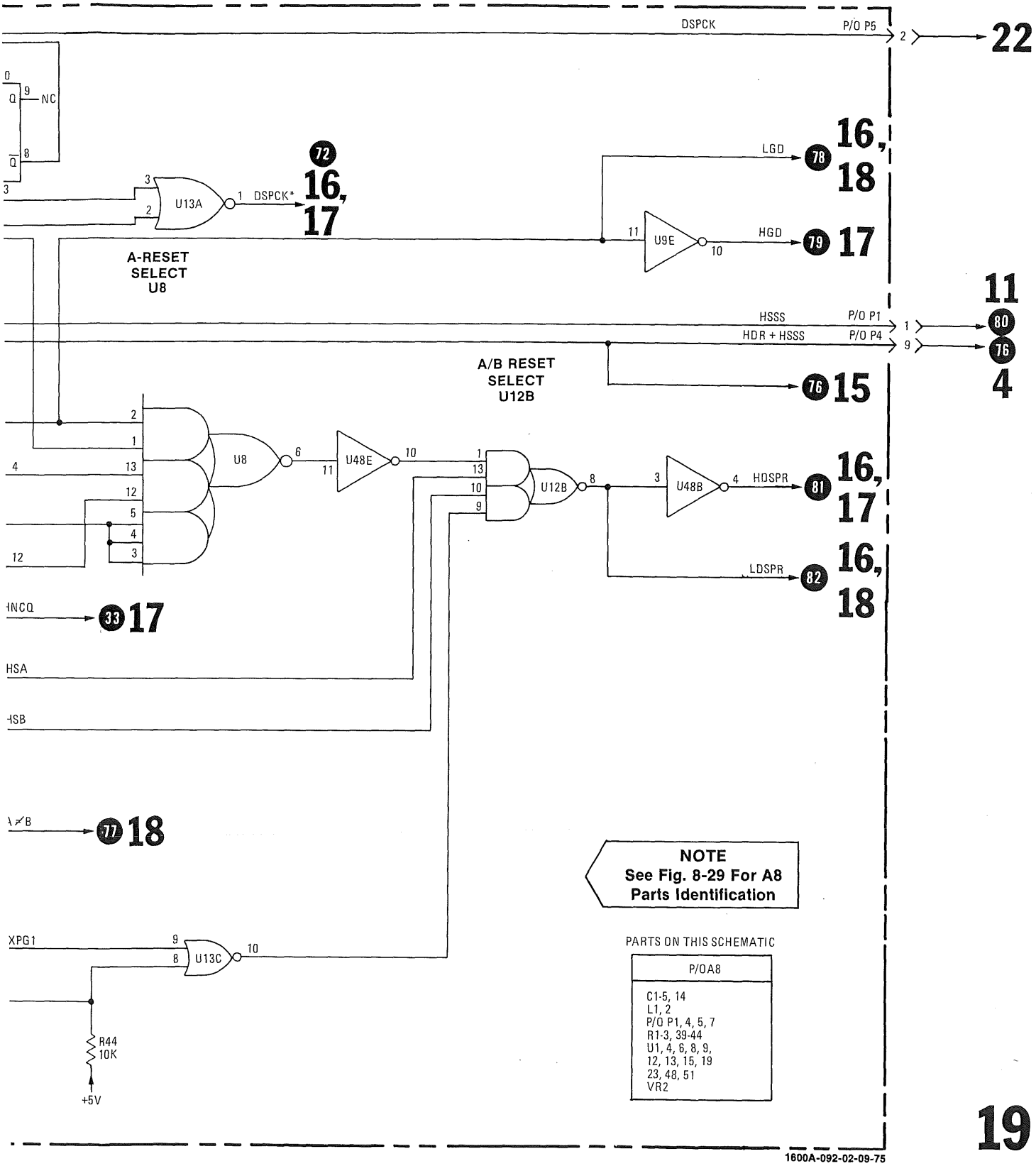
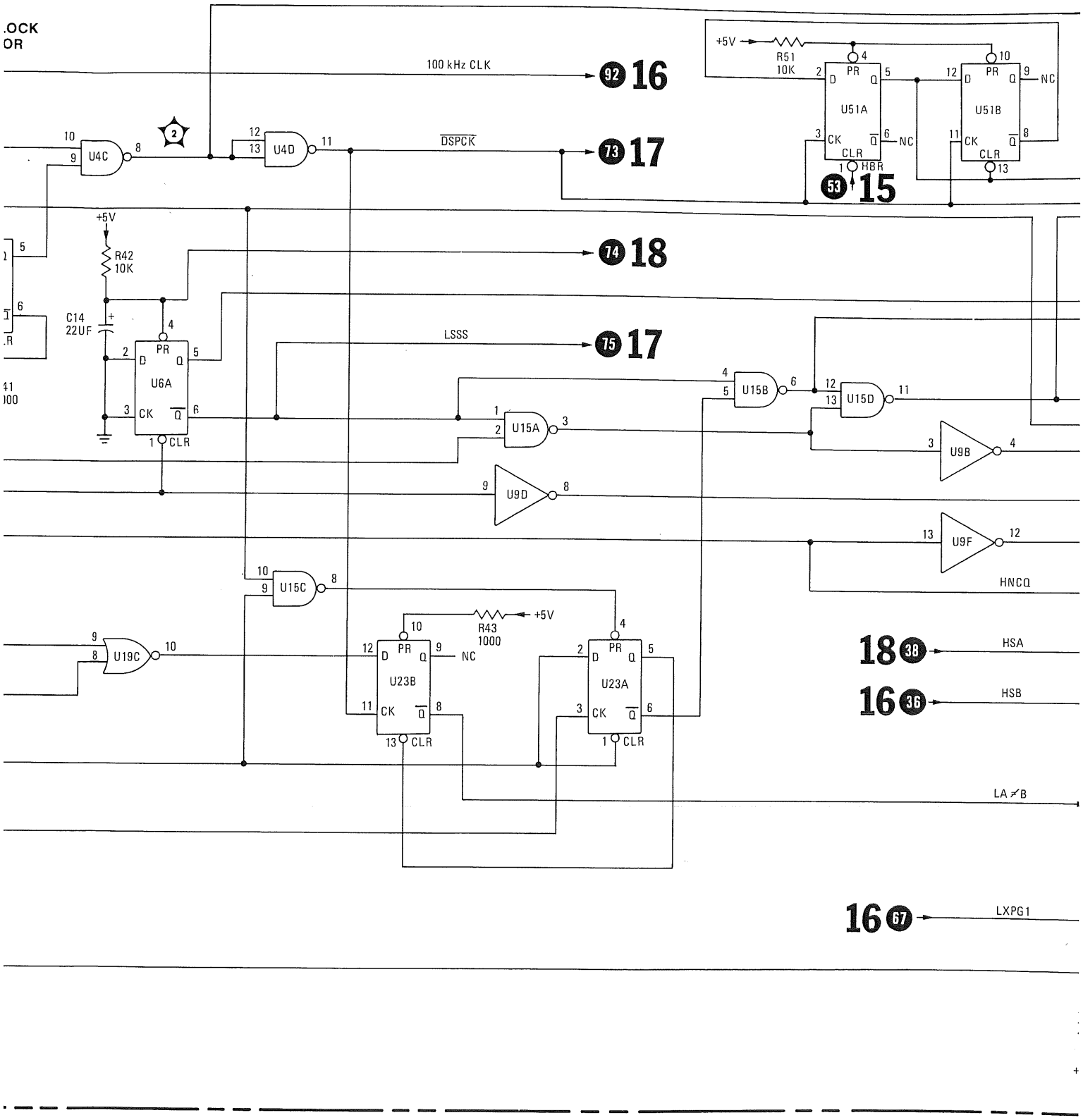
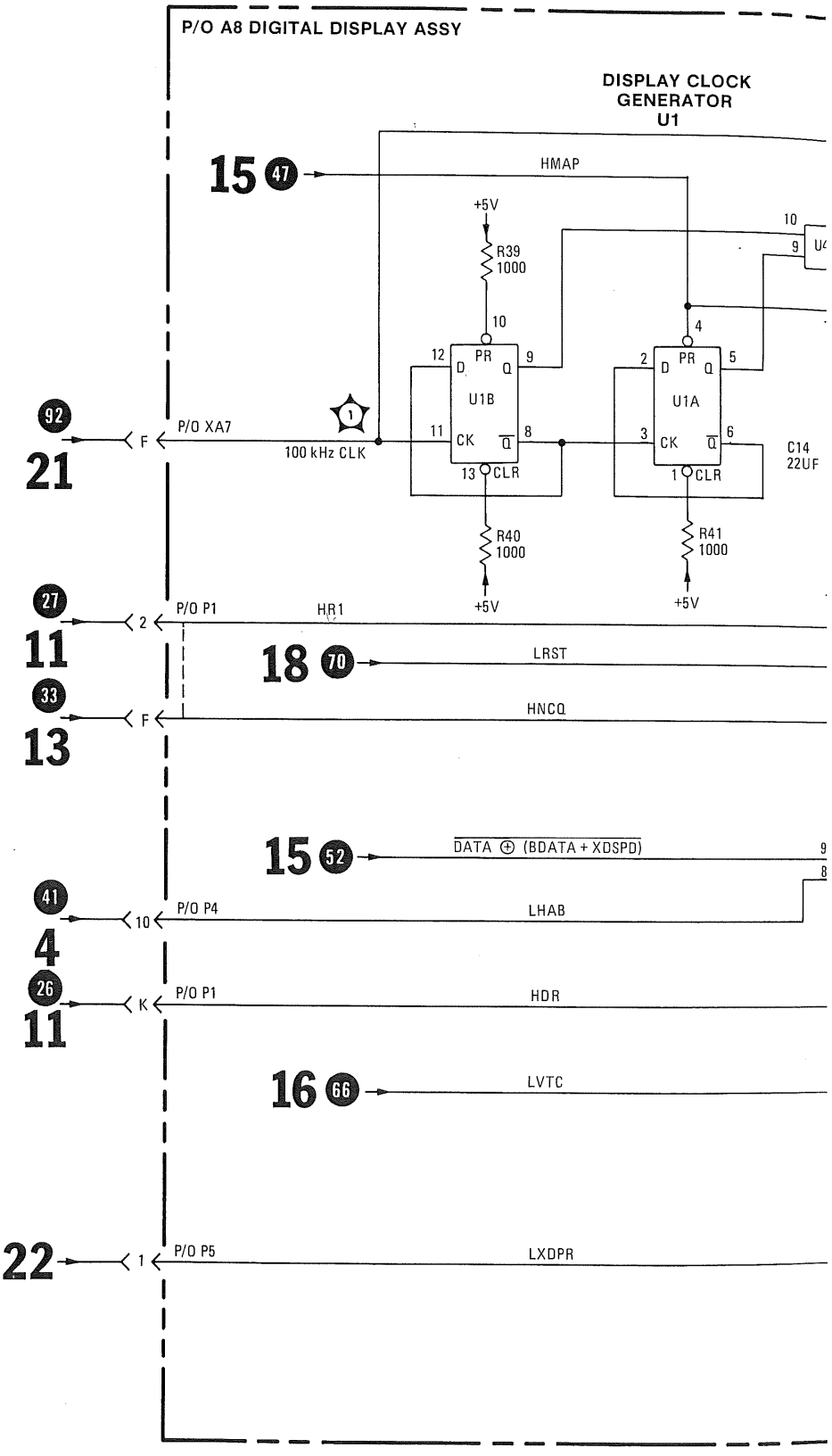


Figure 8-33.
Schematic 19, Display Clock Generator and Display Reset (Sheet 2 of 2)


.OCK
OR
100 kHz CLK
92 16
U4C
U4D
DSPCK
73 17
+5V
R51
10K
U51A
U51B
NC
HBR
53 15
+5V
R42
10K
74 18
C14
22UF
U6A
PR
CLR
LSSS
75 17
U15A
U15B
U15D
U9B
U9D
U9F
HNCQ
U15C
U19C
+5V
R43
1000
U23B
U23A
18 38 HSA
16 36 HSB
LA ⁄ B
16 67 LXPG1


P/O A8 DIGITAL DISPLAY ASSY
DISPLAY CLOCK GENERATOR U1
15 47
HMAP
+5V
R39 1000
10
12
PR
D
Q
9
U1B
11
CK
Q
8
13
CLR
R40 1000
+5V
4
2
PR
D
Q
5
U1A
3
CK
Q
6
1
CLR
R41 1000
+5V
C14 22UF
92
21
F
P/O XA7
1
100 kHz CLK
27
11
2
P/O P1
HR1
18 70
LRST
33
13
F
HNCQ
15 52
DATA ⊕ (BDATA + XDSPD)
41
4
10
P/O P4
LHAB
26
11
K
P/O P1
HDR
16 66
LVTC
22
1
P/O P5
LXDPR

SCHEMATIC 20
TRUTH TABLES

A7U7/MULTIPLEXER A7U8 TRUTH TABLE

INPUT		OUTPUT	
VM3	VM2	VM1	VM0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

HORIZONTAL/VERTICAL DECODER TRUTH TABLE

LMAP	LXPMP	DECODER OUTPUTS
0	0	MDO-5, MD 8-13
0	1	MD2-7, MD10-15
1	1	HM1-5, VM0-5

HIRIZONTAL ROM A7U14 TRUTH TABLE

INPUTS						OUTPUTS*				INPUTS						OUTPUTS*			
HTBD	HOCT	H3	H2	H1	H0	HM4	HM3	HM2	HM1	HBTD	HOCT	H3	H2	H1	H0	HM4	HM3	HM2	HM1
0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	1	1	0	1
0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	1	1	0	0
0	0	0	0	1	0	1	1	0	0	1	0	0	0	1	0	1	0	1	1
0	0	0	0	1	1	1	0	1	1	1	0	0	0	1	1	1	0	1	0
0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	1	0	0	0	1	0	0	1	0	1	0	1	1	1
0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	1	1	0
0	0	0	1	1	1	0	1	1	0	1	0	0	1	1	1	0	1	0	1
0	0	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	1
0	0	1	0	0	1	0	0	1	1	1	0	1	0	0	1	0	0	1	0
0	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1	0	0	0	0
0	0	1	1	0	0	1	1	1	1	1	0	1	1	0	0	1	1	1	0
0	0	1	1	0	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1
0	0	1	1	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	0
0	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	1	0	1	1
0	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	1	1	1
0	1	0	0	0	1	1	1	0	1	1	1	0	0	0	1	1	1	1	0
0	1	0	0	1	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1
0	1	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	0	1	1
0	1	0	1	0	0	1	0	0	1	1	1	0	1	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1	0	0	1
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0	1	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1
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0	1	1	0	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	1
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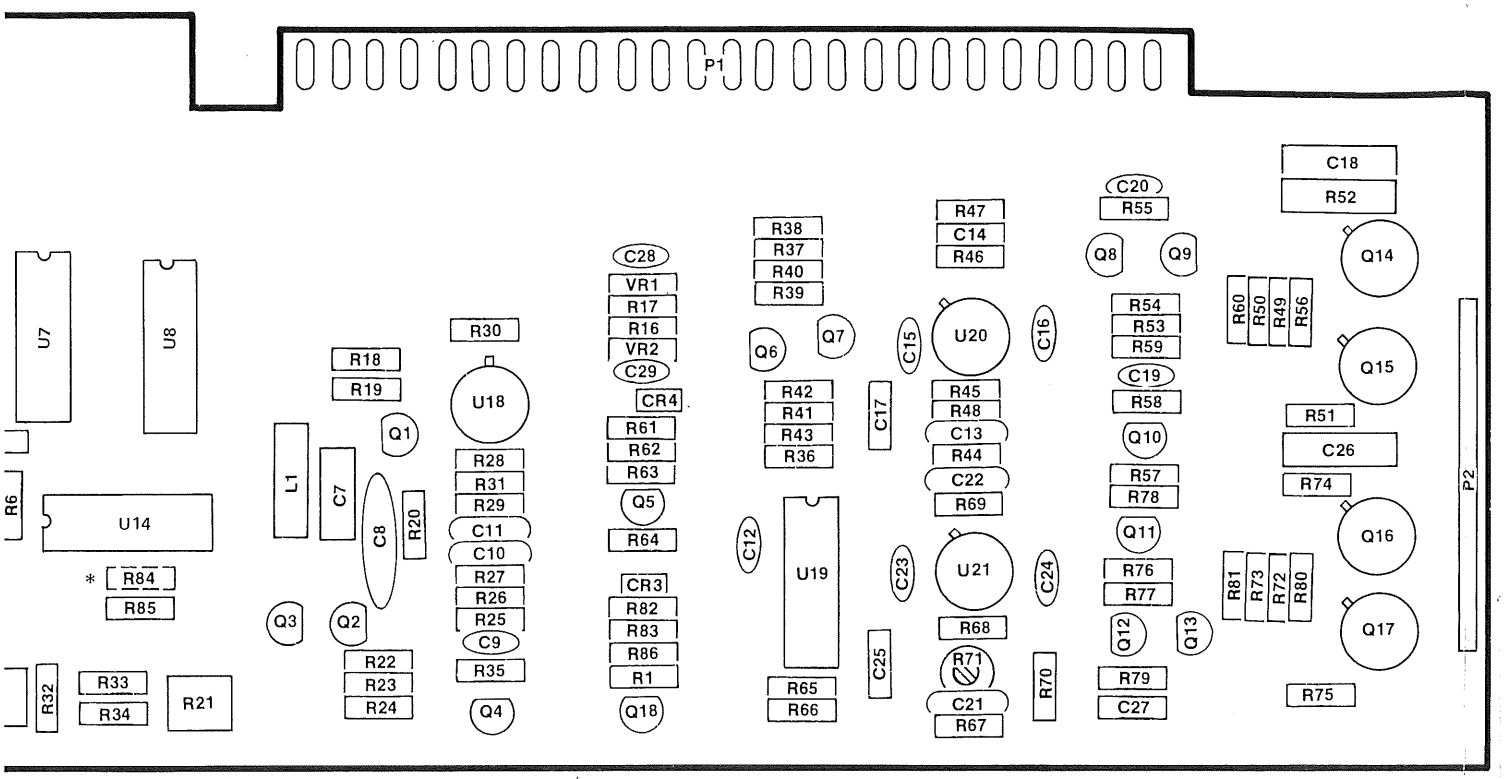
0	1	1	1	0	1	1	1	0	1	1	1	1	1	0	1	1	1	1	0
0	1	1	1	1	0	1	1	0	0	1	1	1	1	1	0	1	1	0	1
0	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1

*HM5 IS GENERATED BY COMPARATOR A7U13.
HM5 = 1 IF HORIZ COUNT ≤ 1011_2
HM5 = 0 IF HORIZ COUNT > 1011_2

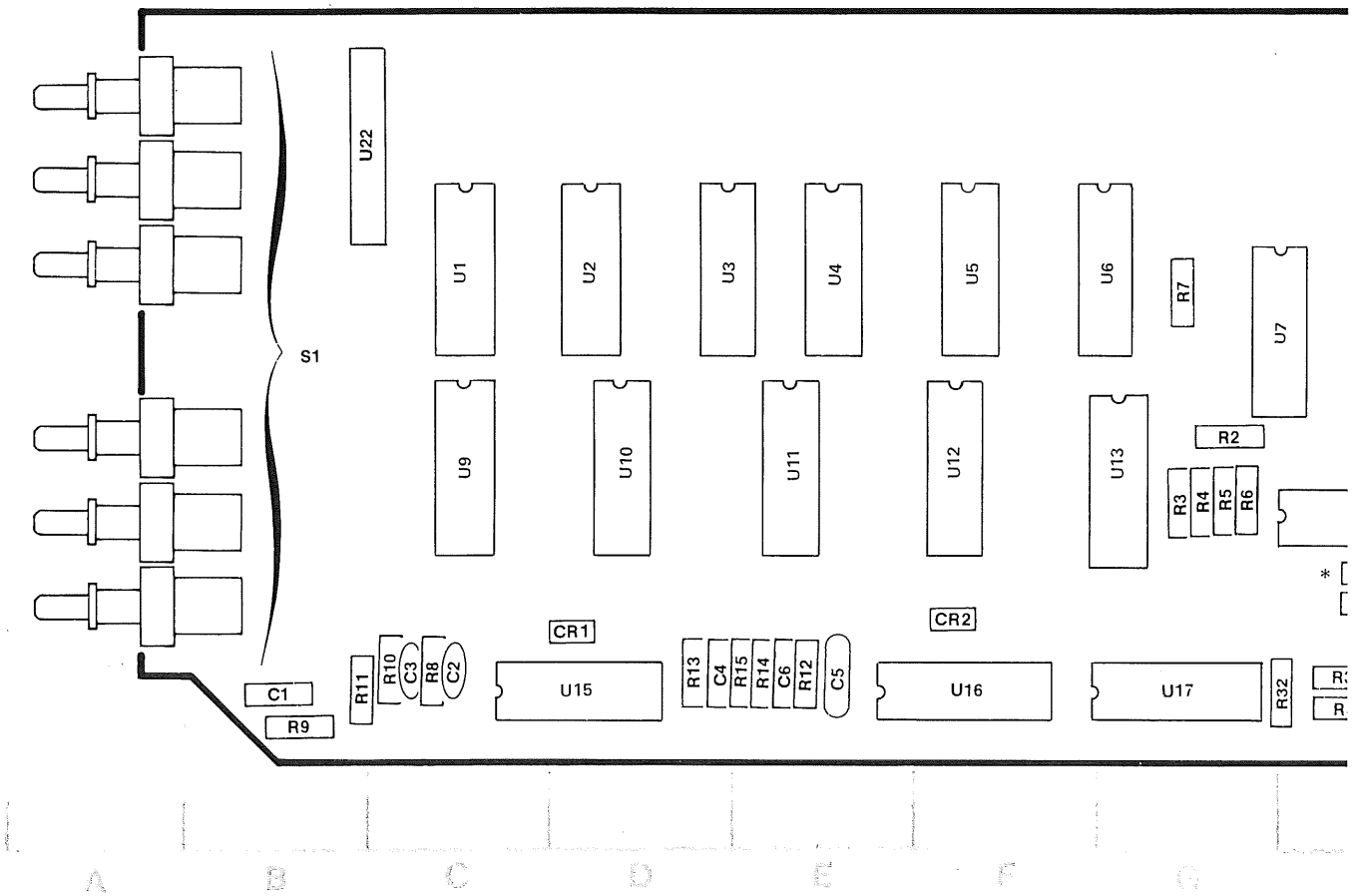
1600A-021-01-09-75

Figure 8-35. Schematic 20, Horizontal and Vertical Decoders and D/A Converters (Sheet 1 of 2)



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
11	C-6	R27	J-5	R44	M-4	R61	K-4	R78	N-5	U8	H-4
12	E-6	R28	J-4	R45	M-4	R62	K-4	R79	N-6	U9	C-4
13	D-6	R29	J-5	R46	M-3	R63	K-4	R80	N-5	U10	D-4
14	E-6	R30	J-4	R47	M-3	R64	K-5	R81	N-5	U11	E-4
15	E-6	R31	J-5	R48	M-4	R65	L-6	R82	K-5	U12	F-4
16	K-4	R32	H-6	R49	N-4	R66	L-6	R83	K-5	U13	G-4
17	K-4	R33	H-6	R50	N-4	R67	M-6	R84*	H-5	U14	H-5
18	I-4	R34	H-6	R51	N-4	R68	M-5	R85	H-5	U15	D-6
19	I-4	R35	J-6	R52	O-3	R69	M-5	R86	K-5	U16	F-6
20	J-5	R36	L-4	R53	N-4	R70	M-6	S1	B-4	U17	G-6
21	H-6	R37	L-3	R54	N-4	R71	M-5	U1	C-3	U18	J-4
22	I-5	R38	L-3	R55	M-3	R72	N-5	U2	D-3	U19	L-5
23	I-6	R39	L-3	R56	N-4	R73	N-5	U3	D-3	U20	M-4
24	I-6	R40	L-3	R57	N-4	R74	N-4	U4	E-3	U21	M-5
25	J-5	R41	L-4	R58	N-4	R75	N-6	U5	F-3	U22	C-3
26	J-5	R42	L-4	R59	N-4	R76	N-5	U6	G-3	VR1	K-3
		R43	L-4	R60	N-4	R77	N-5	U7	H-4	VR2	K-4

Parts Identification, Board Assy A7



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-6	C17	L-4	CR4	K-4	Q13	N-5	R11	C-6
C2	C-6	C18	O-3	L1	I-4	Q14	O-3	R12	E-6
C3	C-6	C19	N-4	P1	K-2	Q15	O-4	R13	D-6
C4	D-6	C20	M-3	P2	O-4	Q16	O-5	R14	E-6
C5	E-6	C21	M-6	Q1	I-4	Q17	O-5	R15	E-6
C6	E-6	C22	M-4	Q2	I-5	Q18	K-6	R16	K-4
C7	I-5	C23	L-5	Q3	I-5	R1	K-6	R17	K-4
C8	I-5	C24	M-5	Q4	J-6	R2	G-4	R18	I-4
C9	J-5	C25	L-5	Q5	K-5	R3	G-5	R19	I-4
C10	J-5	C26	O-4	Q6	K-4	R4	G-5	R20	J-5
C11	J-5	C27	N-6	Q7	L-4	R5	G-5	R21	H-6
C12	K-5	C28	K-3	Q8	M-3	R6	G-5	R22	I-5
C13	M-4	C29	K-4	Q9	N-3	R7	G-3	R23	I-6
C14	M-3	CR1	D-5	Q10	N-4	R8	C-6	R24	I-6
C15	L-4	CR2	F-5	Q11	N-5	R9	B-6	R25	J-5
C16	M-4	CR3	K-5	Q12	N-5	R10	C-6	R26	J-5

Figure 8-34. Parts Iden

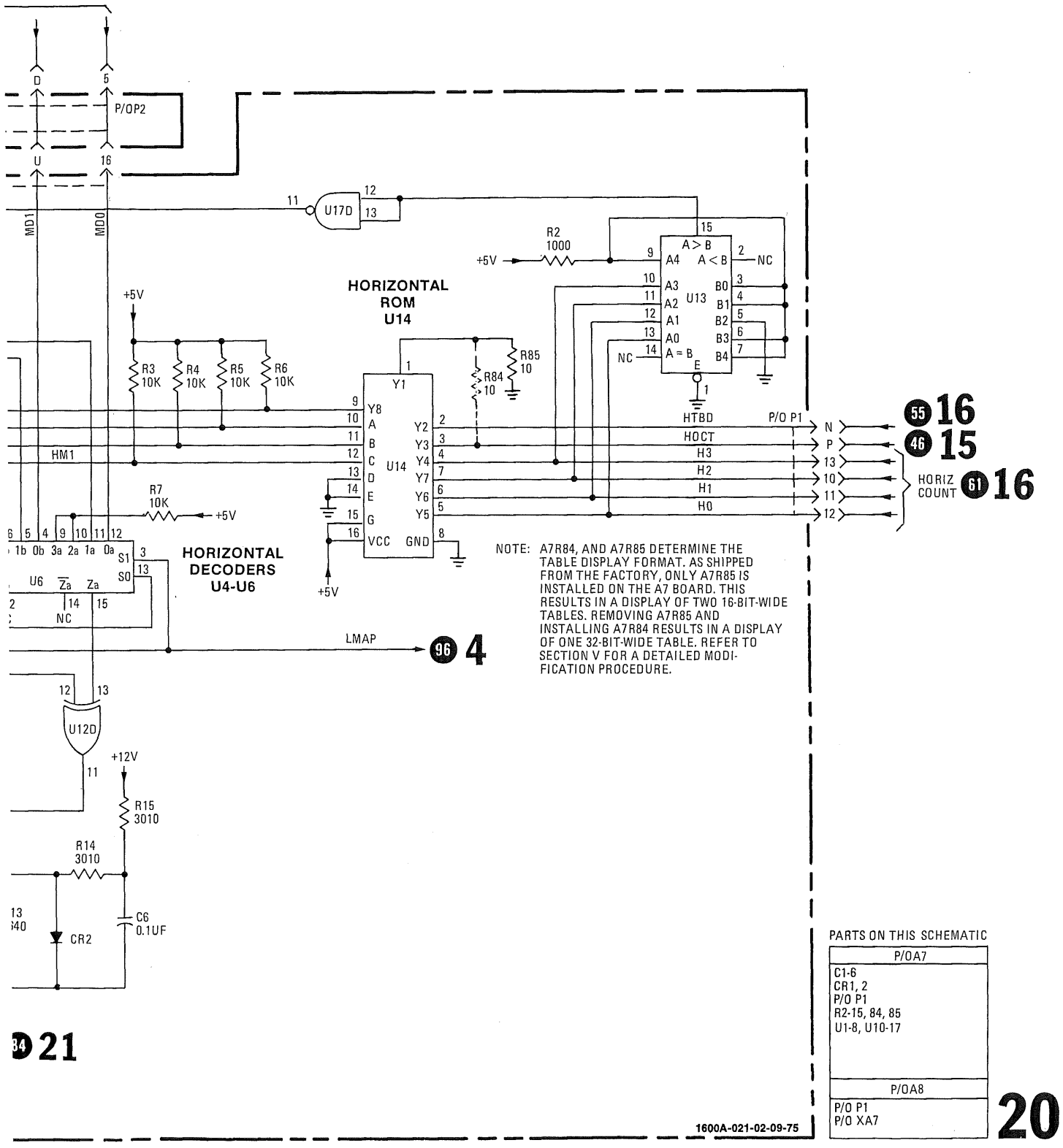
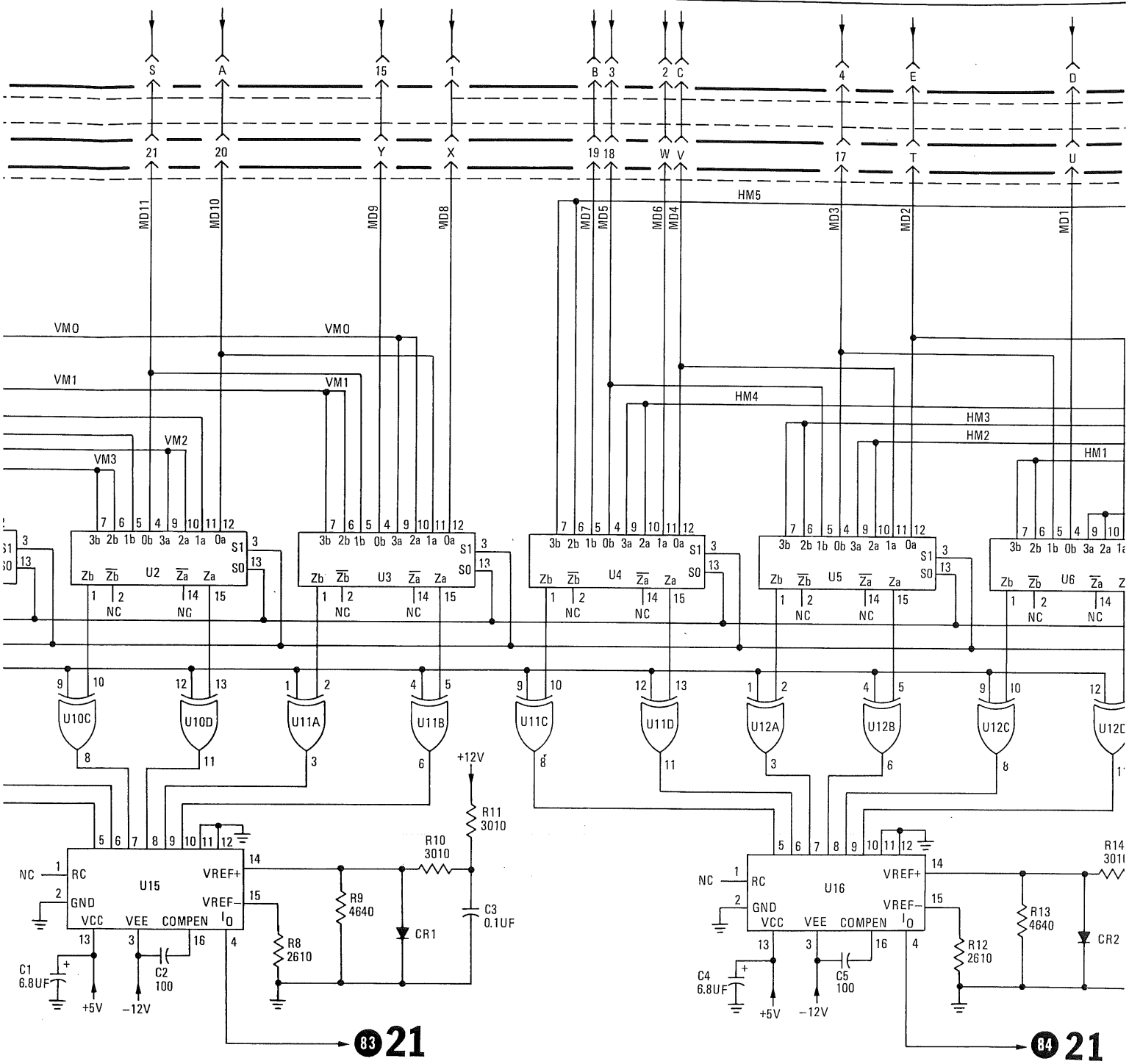
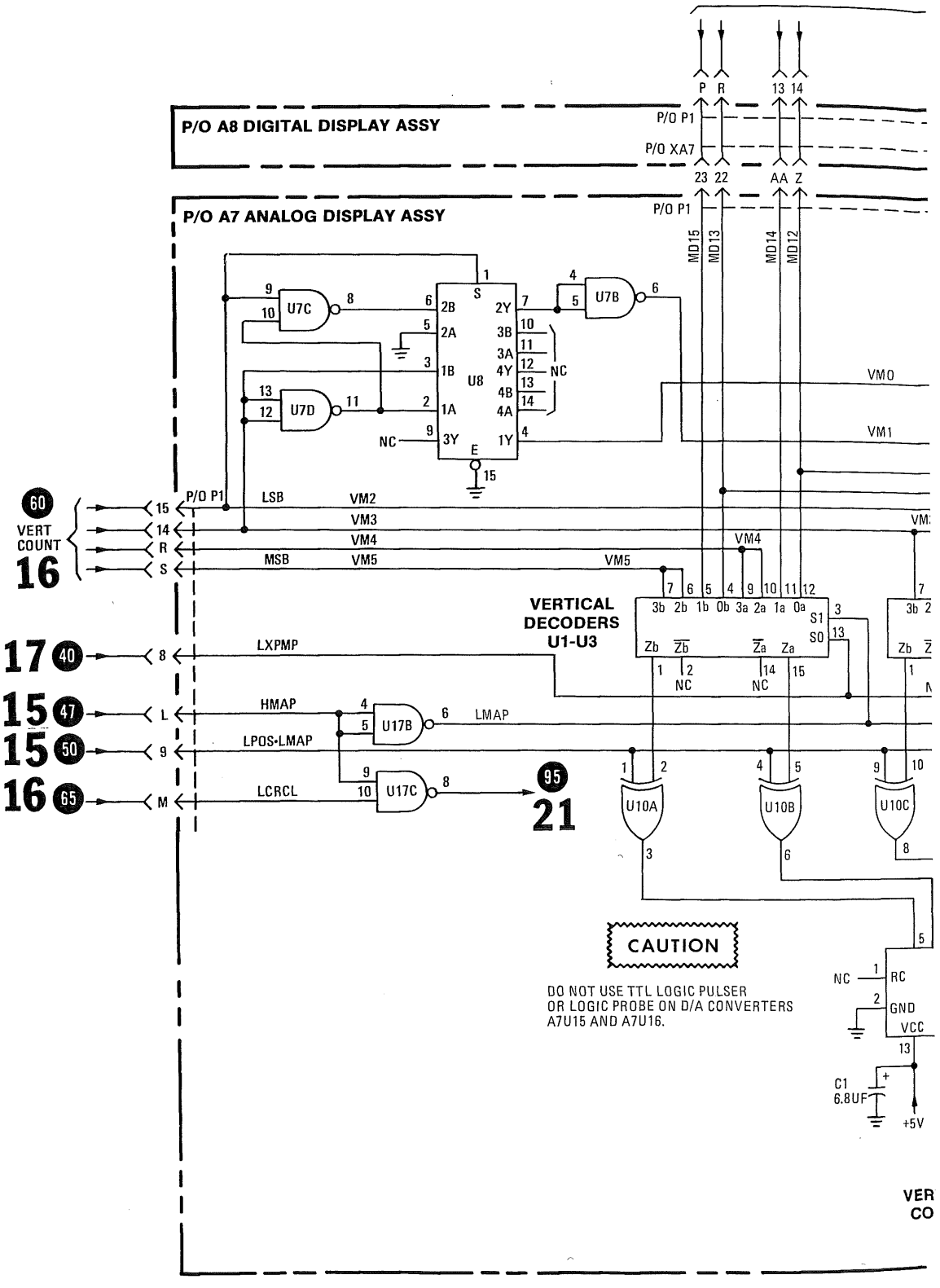


Figure 8-35.
Schematic 20, Horizontal and Vertical Decoders and D/A Converters (Sheet 2 of 2)



VERTICAL D/A CONVERTER U15

HORIZONTAL D/A CONVERTER U16


P/O A8 DIGITAL DISPLAY ASSY
P/O A7 ANALOG DISPLAY ASSY
P/O P1
P/O XA7
P R 13 14
23 22 AA Z
MD15 MD13 MD14 MD12
U8
U7B
U7C
U7D
VMO
VM1
VM2
VM3
VM4
VM5
LSB
MSB
60
VERT COUNT
16
17 40
15 47
15 50
16 65
LXPMP
HMAP
LPOS·LMAP
LCRCL
LMAP
U17B
U17C
95
21
VERTICAL DECODERS U1-U3
U10A
U10B
U10C
CAUTION
DO NOT USE TTL LOGIC PULSER OR LOGIC PROBE ON D/A CONVERTERS A7U15 AND A7U16.
RC
GND
VCC
C1 6.8UF
+5V

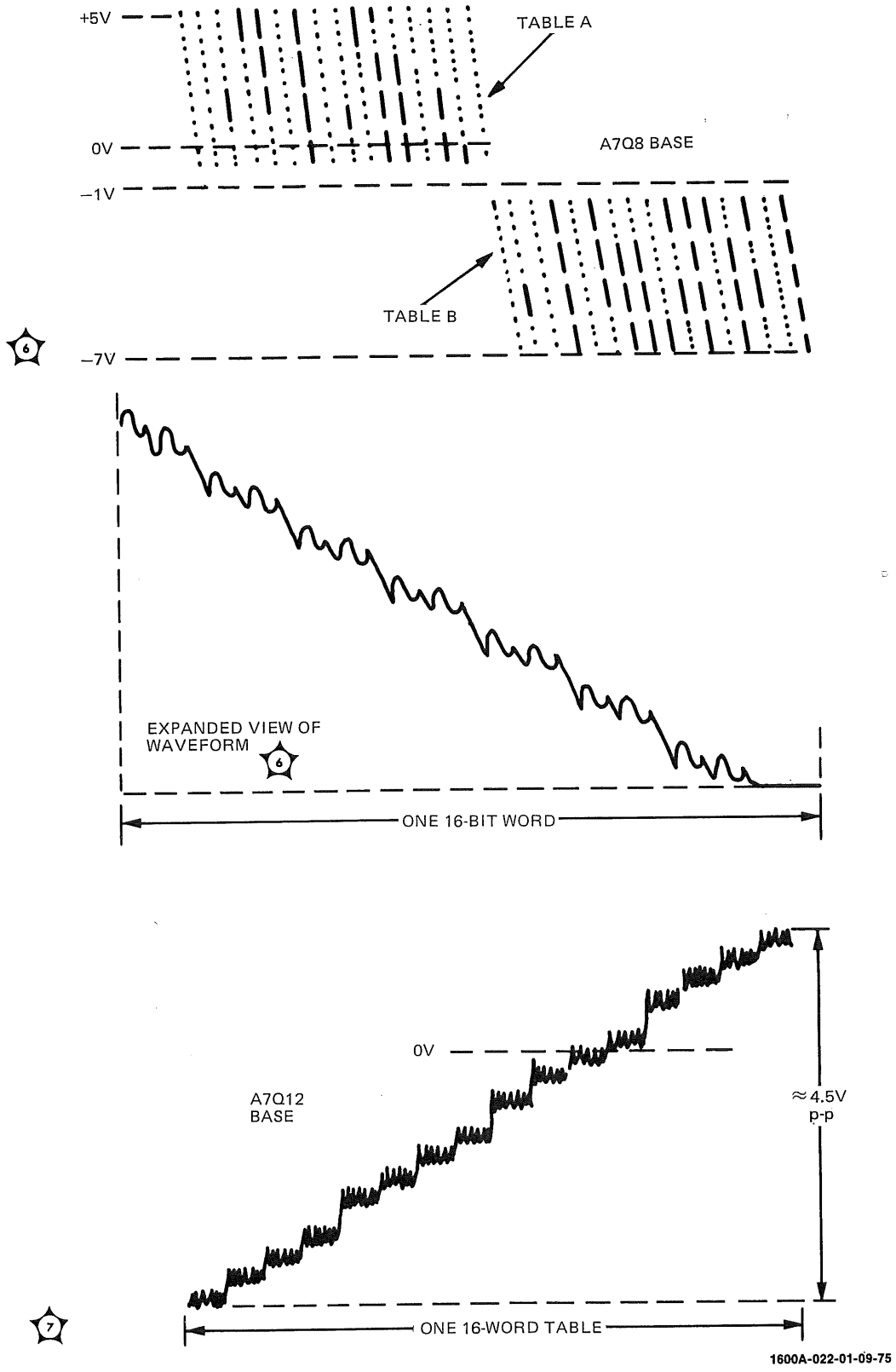
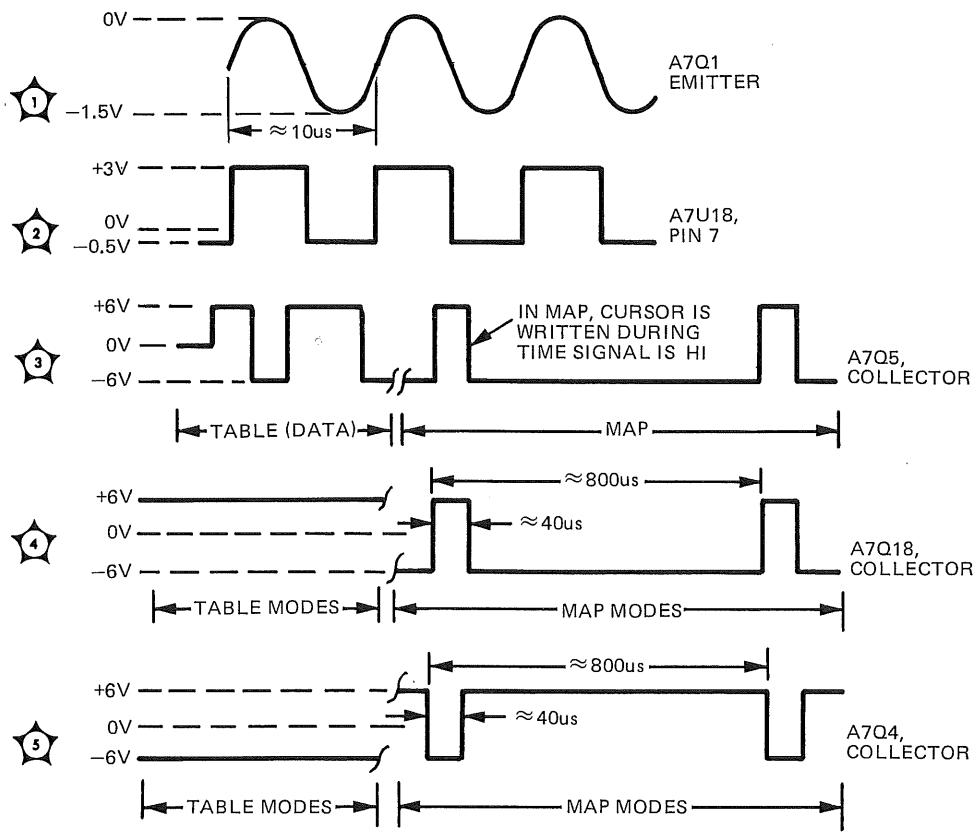


Figure 8-36. Schematic 21. Analog Output Amplifiers (Sheet 1 of 2)

SCHEMATIC 21
WAVEFORM MEASUREMENT CONDITIONS

Set Model 1600A controls as follows:

SAMPLE MODE	SGL
DISPLAY MODE	TABLE A & B
TRIGGER MODE	START DSPL
WORD	ON
DELAY	OFF
THUMBWHEELS	ALL 0's
COLUMN BLANKING	FULL CCW
LOGIC	POS
BYTE	4 BIT
INTENSITY	12 O'CLOCK
FOCUS	12 O'CLOCK



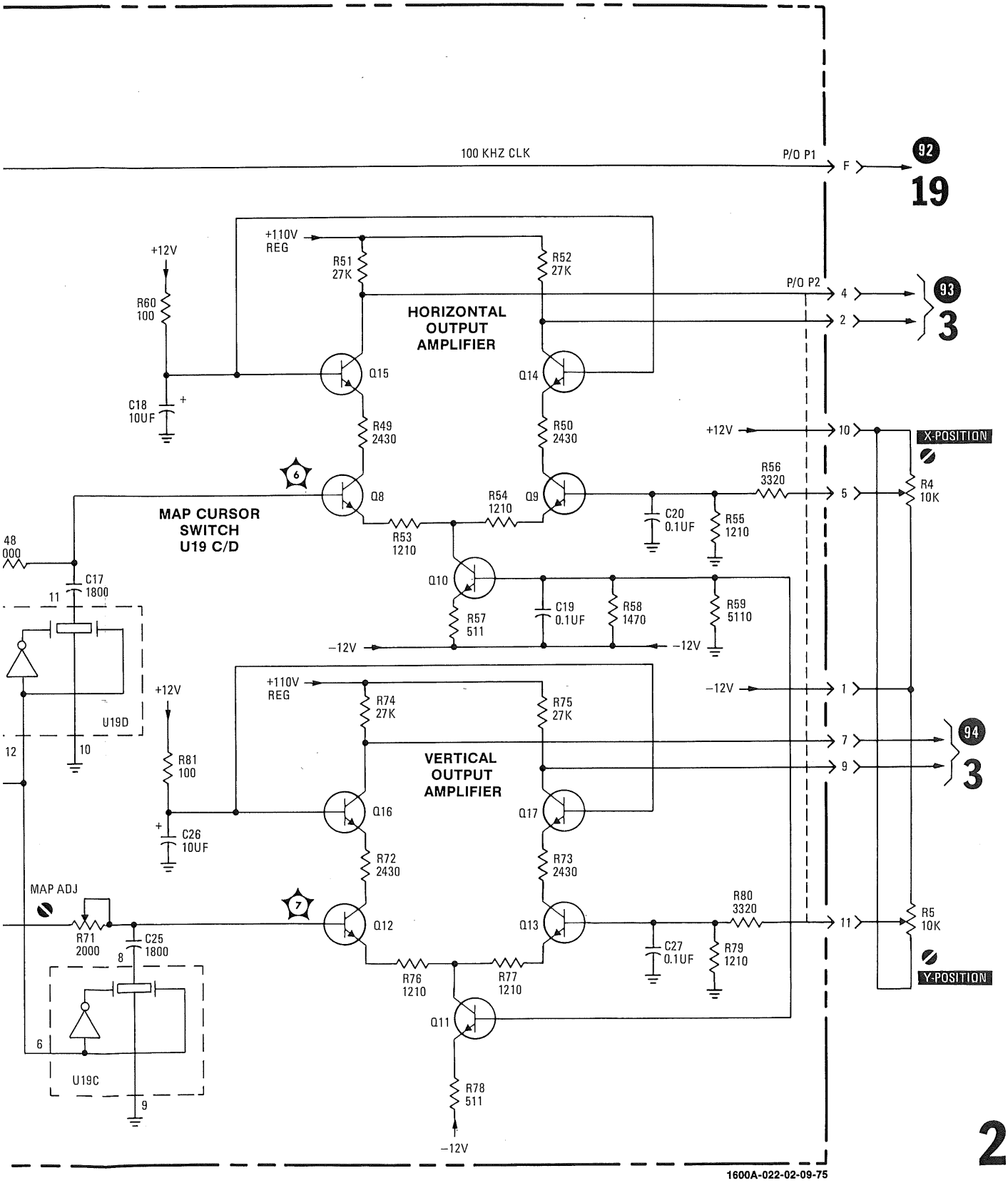
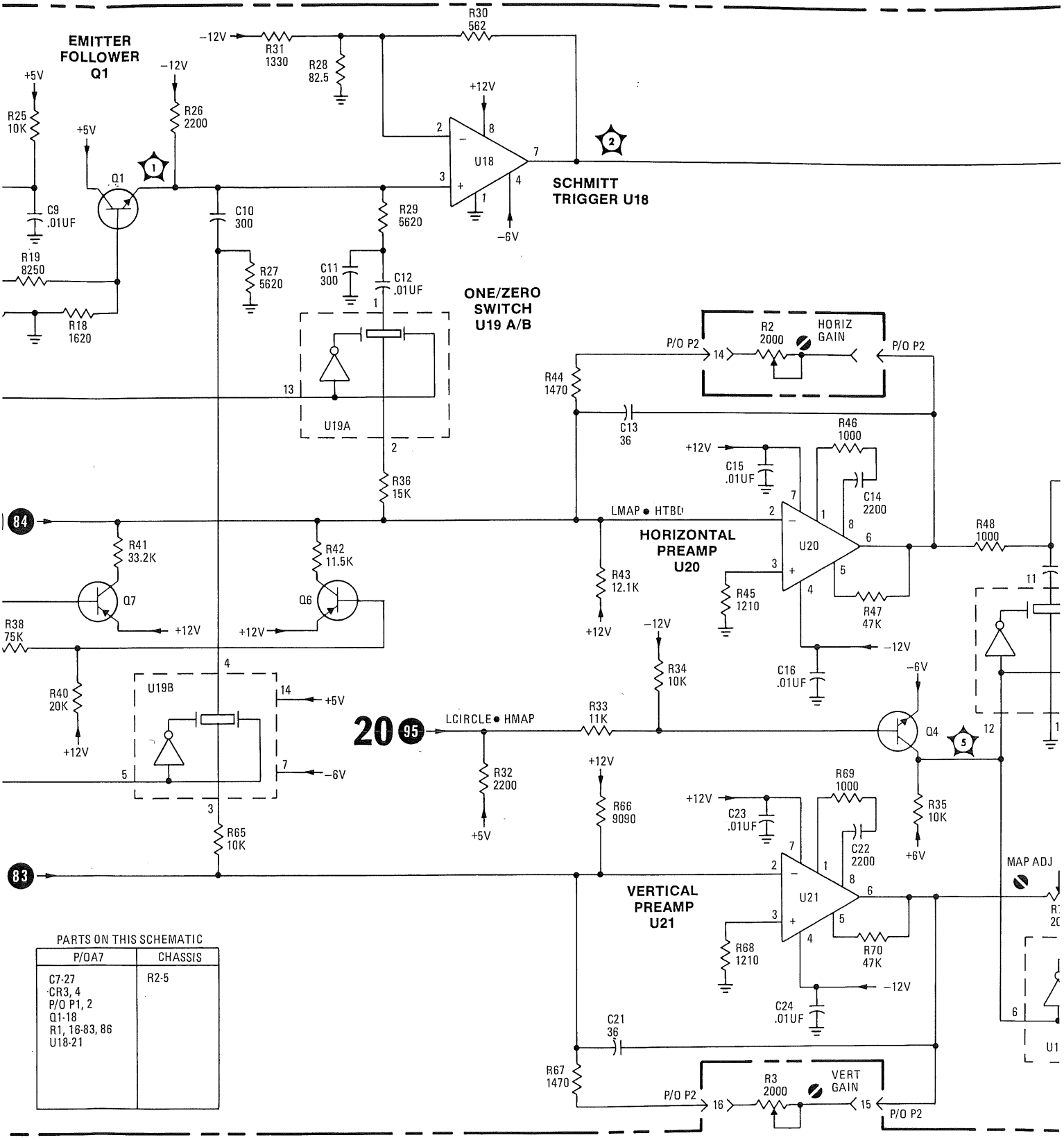
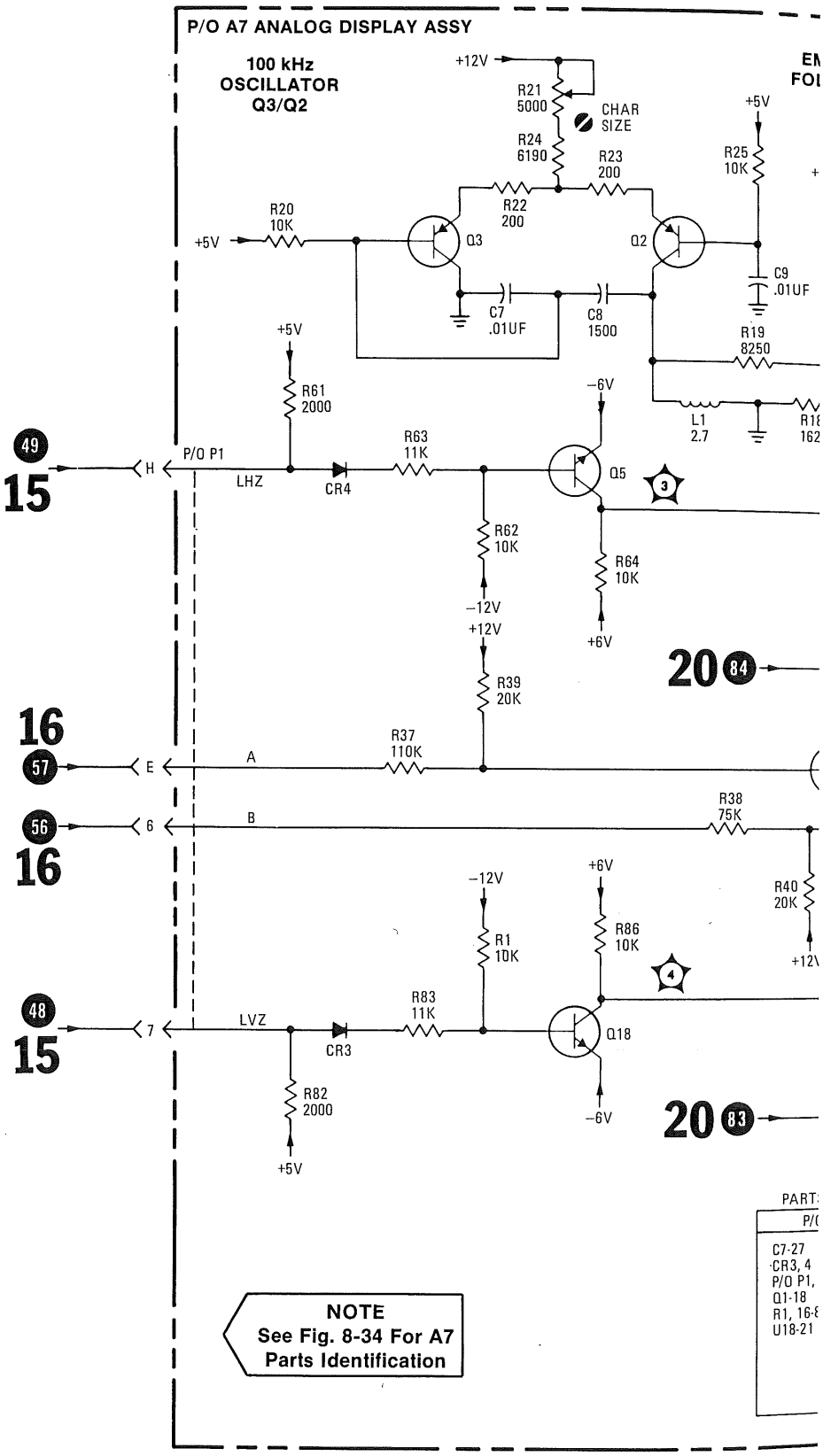


Figure 8-36.
Schematic 21. Analog Output Amplifiers (Sheet 2 of 2)



PARTS ON THIS SCHEMATIC

P/OA7	CHASSIS
C7-27 CR3, 4 P/O P1, 2 Q1-18 R1, 16-83, 86 U18-21	R2-5


P/O A7 ANALOG DISPLAY ASSY
100 kHz
OSCILLATOR
Q3/Q2
+12V
R21
5000
CHAR
SIZE
R24
6190
R23
200
R22
200
R20
10K
+5V
Q3
Q2
+5V
R25
10K
C9
.01UF
C7
.01UF
C8
1500
R19
8250
L1
2.7
+5V
R61
2000
-6V
49
15
H
P/O P1
LHZ
CR4
R63
11K
Q5
3
R62
10K
R64
10K
-12V
+12V
+6V
R39
20K
20 84
16
57
E
A
R37
110K
56
6
B
R38
75K
16
-12V
+6V
R40
20K
R1
10K
R86
10K
4
48
15
7
LVZ
CR3
R83
11K
Q18
R82
2000
+5V
-6V
20 83
NOTE
See Fig. 8-34 For A7
Parts Identification

J6 INTERCONNECTION TABLE

A8P5 PIN NO.	A8P6 PIN NO.	SIGNAL
5		GND
2		50 KHZ CLK
15		LXPG3
12		LWEX
10		LWDX
	6	XH0
	5	XH1
	4	XH2
	3	XH3
	12	XV0
	9	XV1
	10	XV2
	8	XV3
14		XDSPD
13		HGDX
	15	LXMR
	13	HXRPR
	14	HMRXT
3		HBRXT
1		LXDPR
6		LXBNK
	7	HBCDX
	1	EDTBS
8		LXPG1
16	2	LXPG2
	11,16	+5V
		L1600(GND)
		SHIELD (GND)

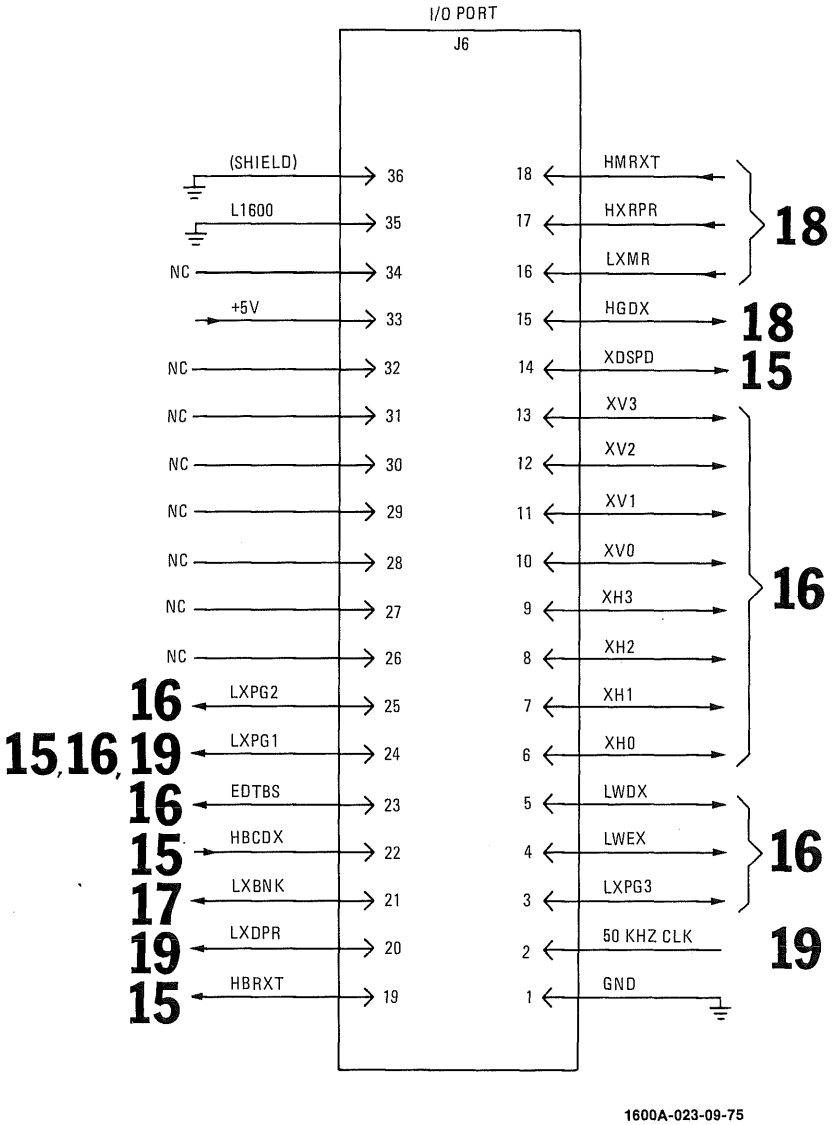
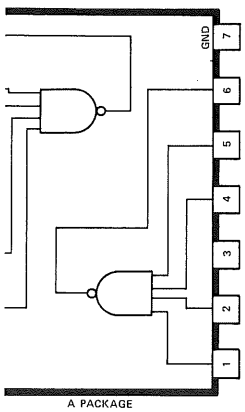


Figure 8-37. Schematic 22, I/O Port J6

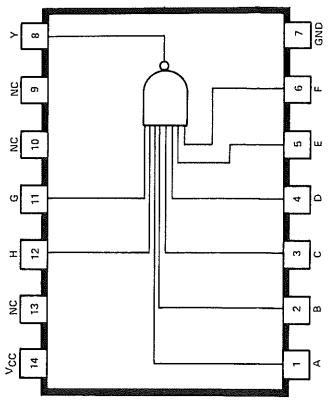
J6 INT

J6 PIN NO.	A8P5 PIN NO.
1	5
2	2
3	15
4	12
5	10
6	
7	
8	
9	
10	
11	
12	
13	
14	14
15	13
16	
17	
18	
19	3
20	1
21	6
22	
23	
24	8
25	16
33	
35	
36	

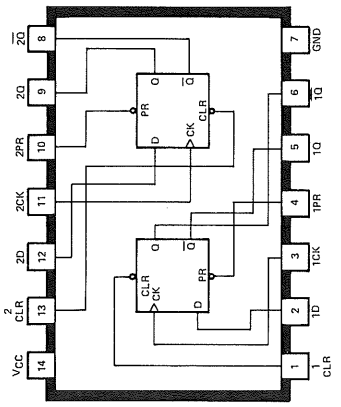


A PACKAGE

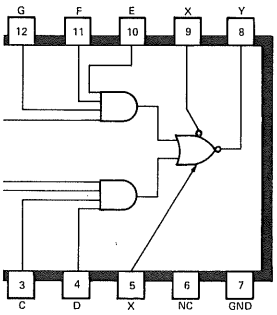
1820-0069
1820-0071
1820-0588
1820-0697



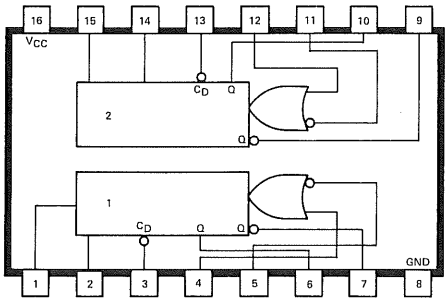
1820-0070
1820-0589



1820-0077



1820-0382



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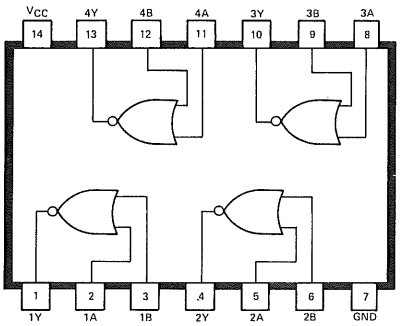

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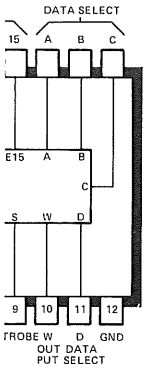
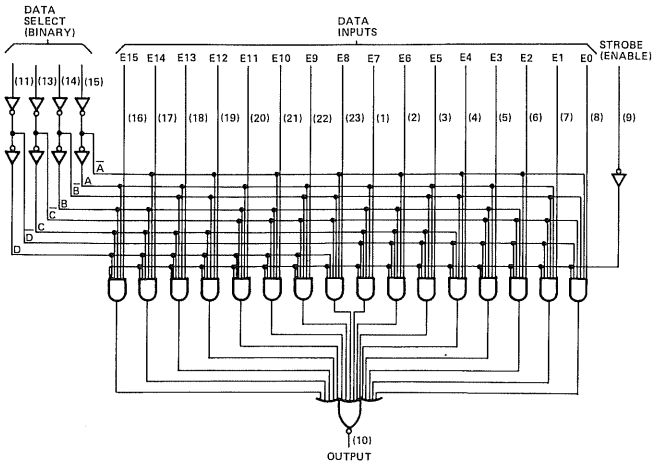


FUNCTION TABLE

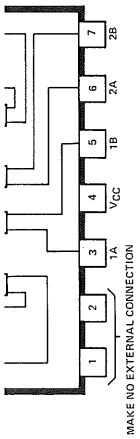
INPUTS					
SELECT				STROBE	OUTPUT
D	C	B	A	S	W
X	X	X	X	H	H
L	L	L	L	L	E0
L	L	L	H	L	E1
L	L	H	L	L	E2
L	L	H	H	L	E3
L	H	L	L	L	E4
L	H	L	H	L	E5
L	H	H	L	L	E6
L	H	H	H	L	E7
H	L	L	L	L	E8
H	L	L	H	L	E9
H	L	H	L	L	E10
H	L	H	H	L	E11
H	H	L	L	L	E12
H	H	L	H	L	E13
H	H	H	L	L	E14
H	H	H	H	L	E15

1820-0640



1600A-085-01-09-75

Figure 8-38.
Integrated Circuit Identification (Sheet 1 of 2)



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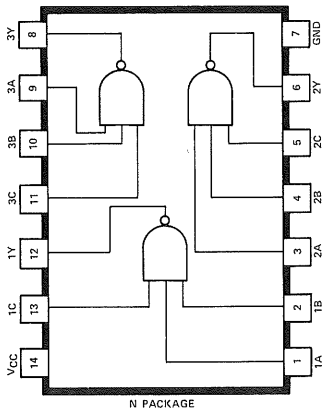

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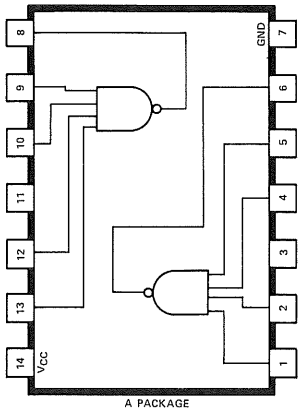

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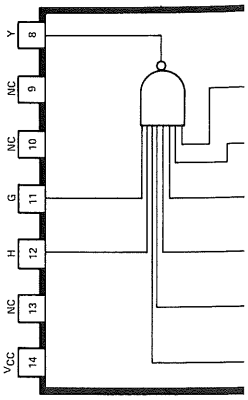

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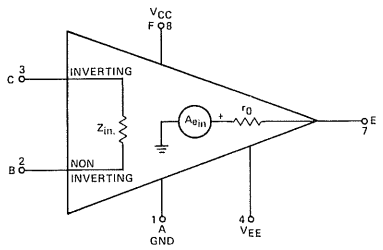

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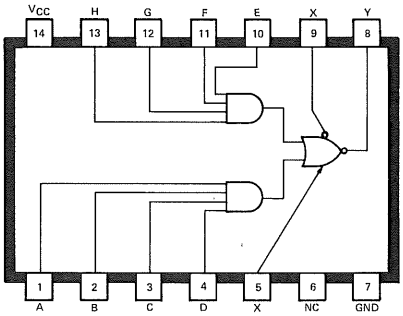

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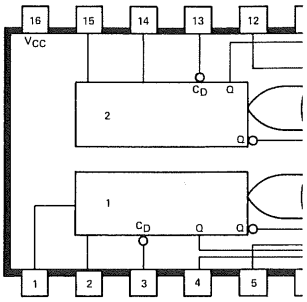

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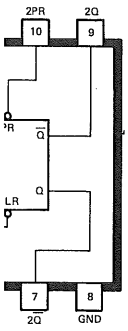

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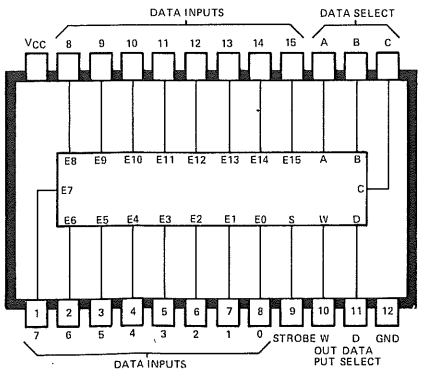

FUNCTION TABLE

INPUTS					
SELECT				STROBE	OUTPUT
D	C	B	A	S	W
X	X	X	X	H	H
L	L	L	L	L	E0
L	L	L	H	L	E1
L	L	H	L	L	E2
L	L	H	H	L	E3
L	H	L	L	L	E4
L	H	L	H	L	E5
L	H	H	L	L	E6
L	H	H	H	L	E7
H	L	L	L	L	E8
H	L	L	H	L	E9
H	L	H	L	L	E10
H	L	H	H	L	E11
H	H	L	L	L	E12
H	H	L	H	L	E13
H	H	H	L	L	E14
H	H	H	H	L	E15

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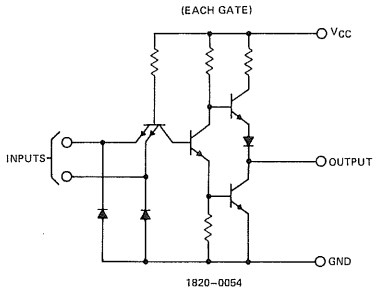

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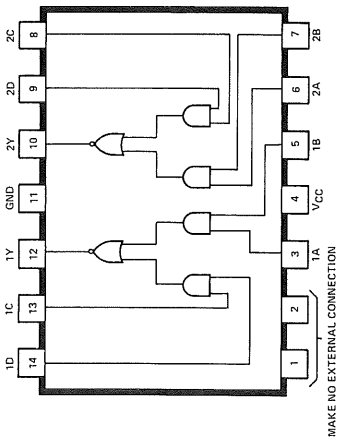

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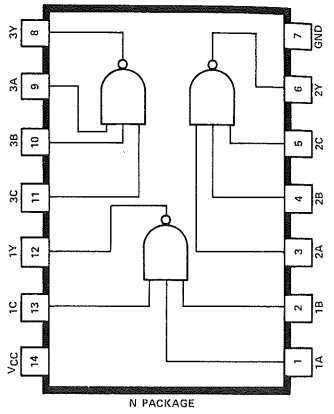

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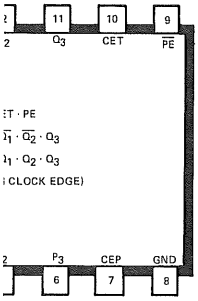

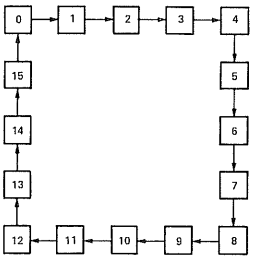

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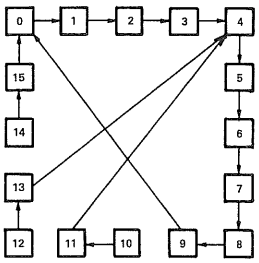

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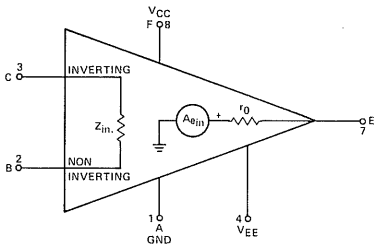

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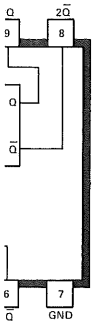

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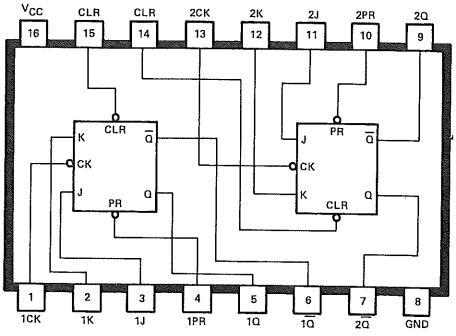

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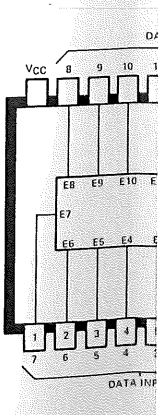

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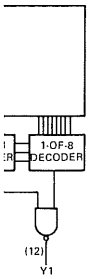

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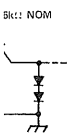

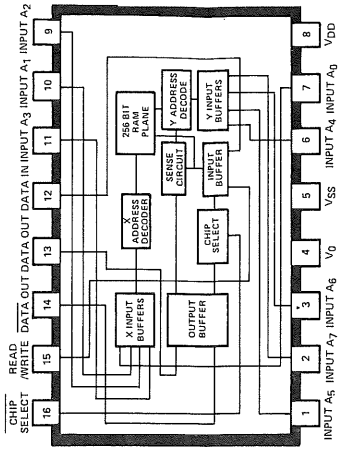

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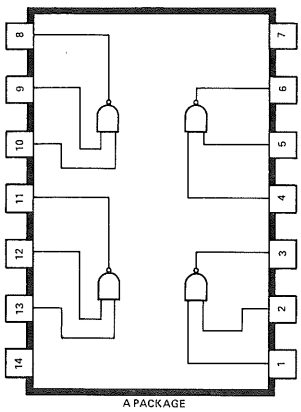

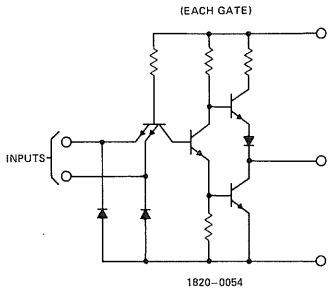

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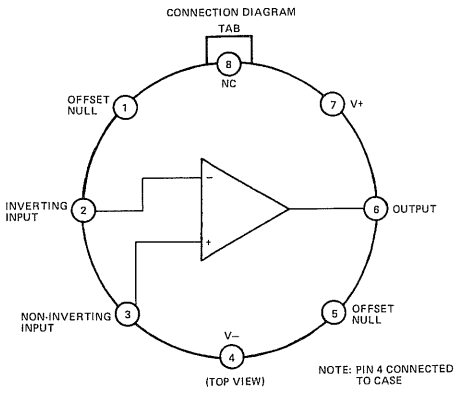

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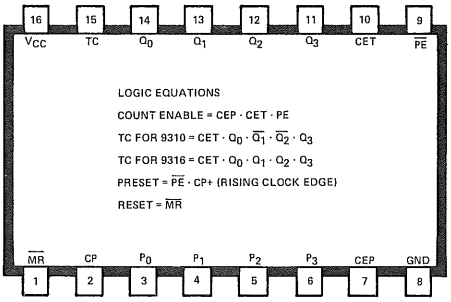

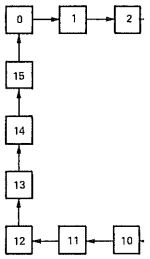

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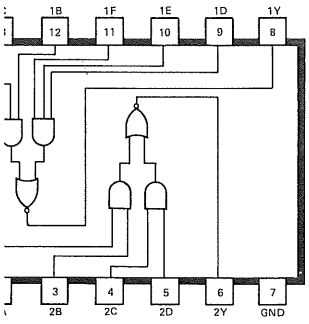

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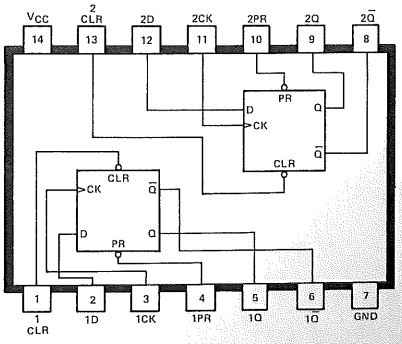

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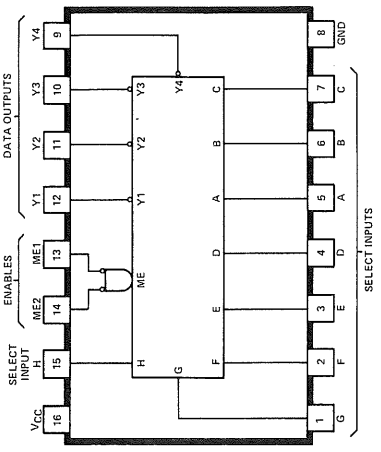

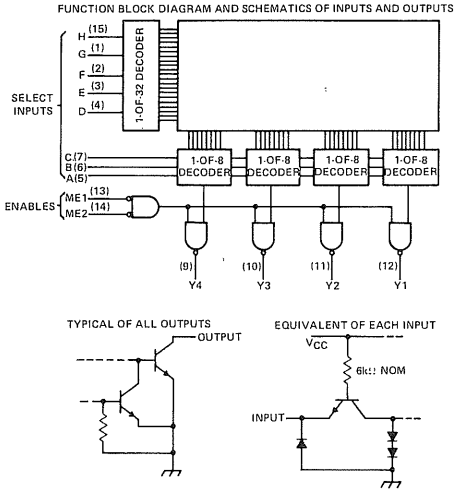

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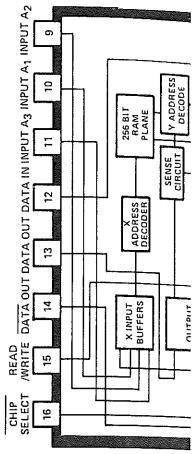

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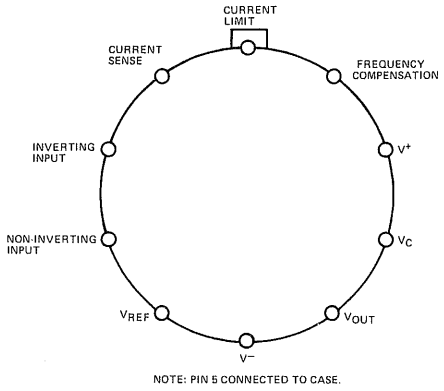

NOTE: PIN 5 CONNECTED TO CASE.

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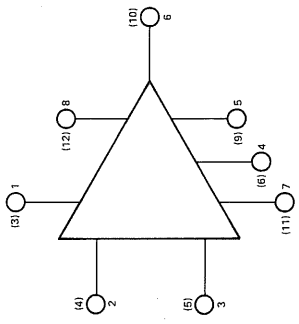

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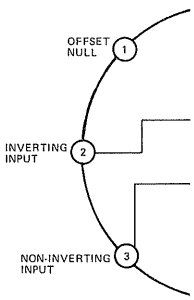

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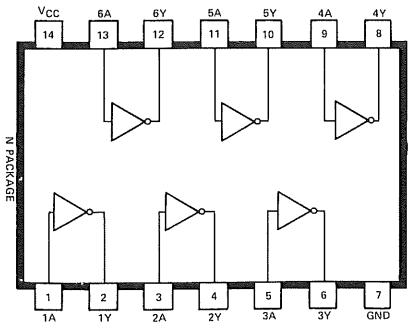

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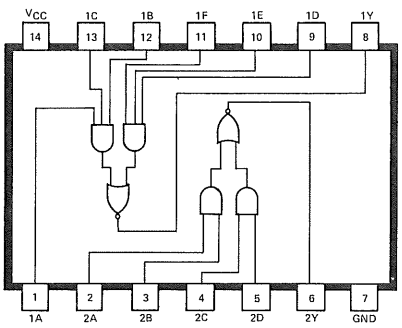

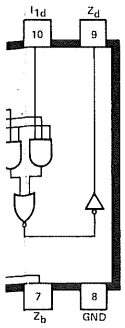

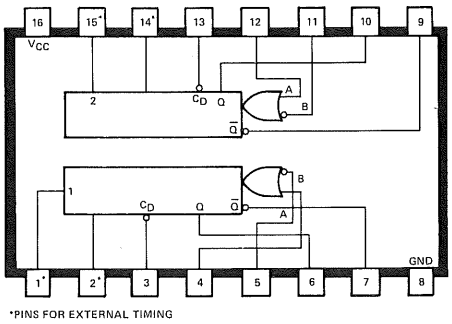

*PINS FOR EXTERNAL TIMING

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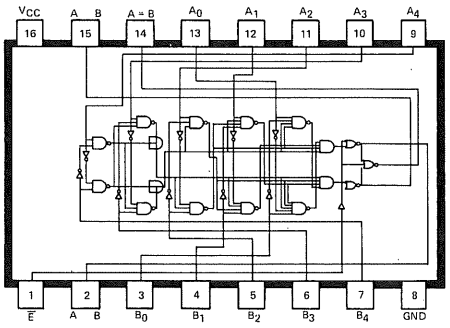

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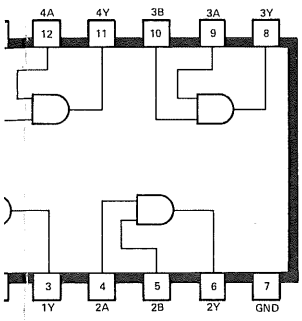

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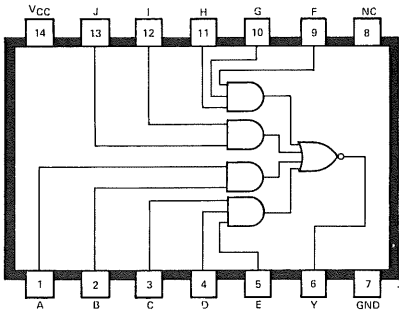

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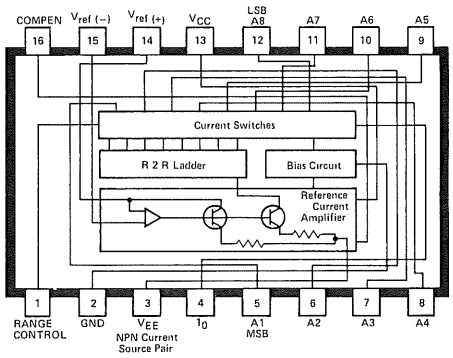

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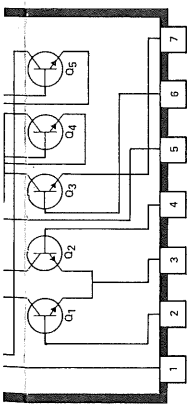

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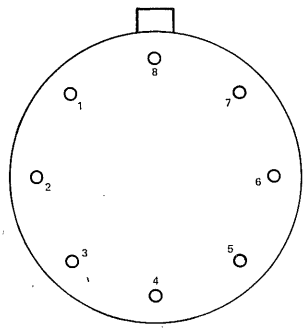

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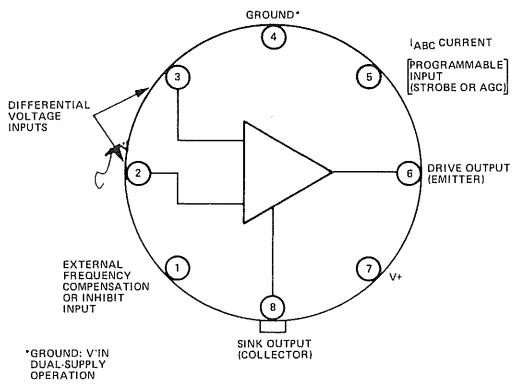
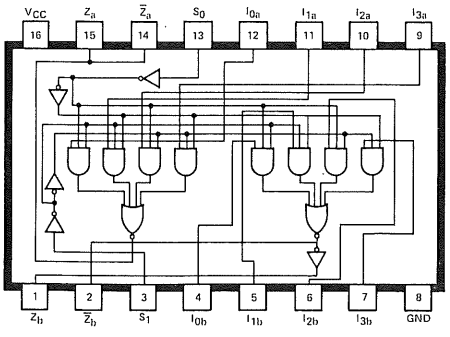


1826-0167

1600A-085-02-09-75

Figure 8-38. Integrated Circuit Identification (Sheet 2 of 2)



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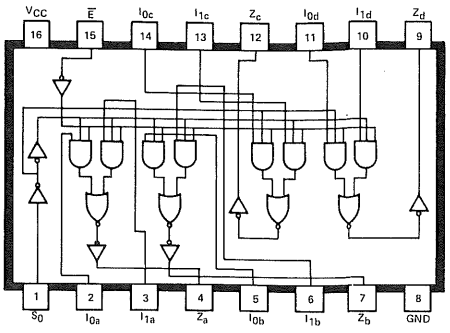
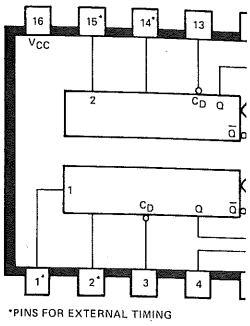
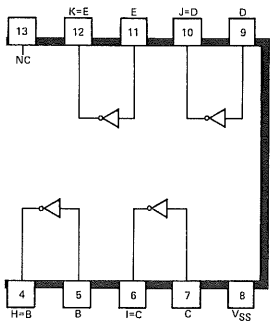


1820-0710



*PINS FOR EXTERNAL TIMING

1820-(



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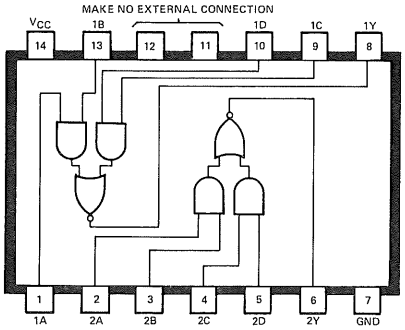

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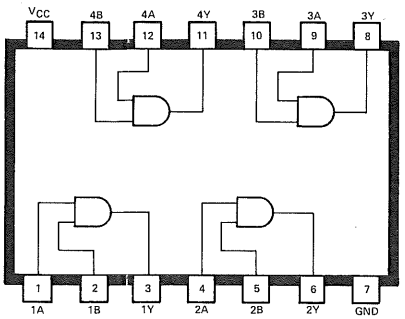

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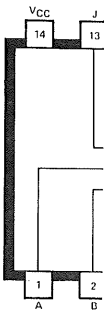

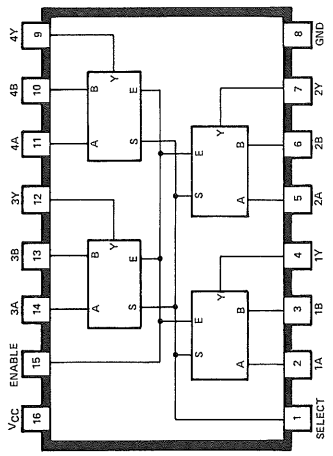

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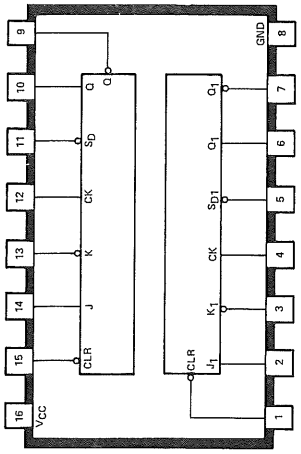

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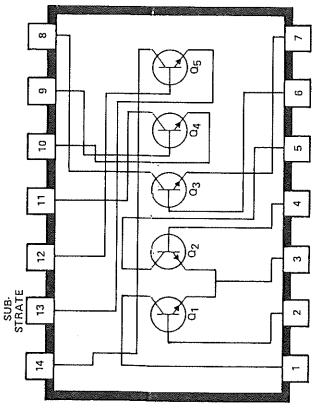

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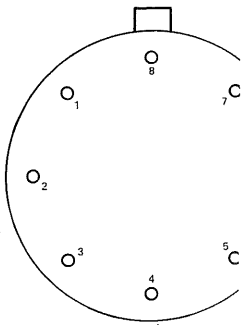

1826-0

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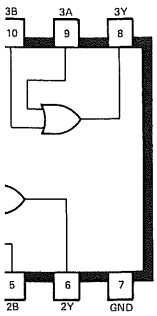

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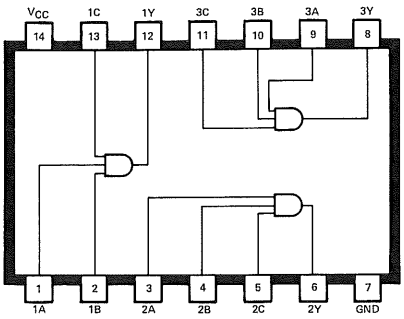

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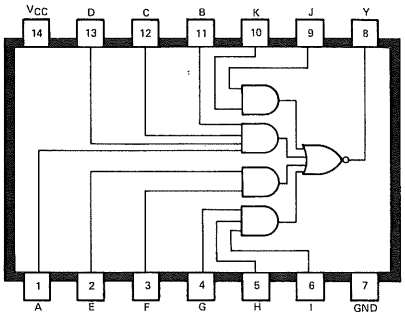

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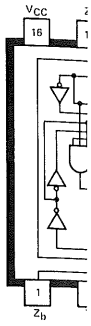
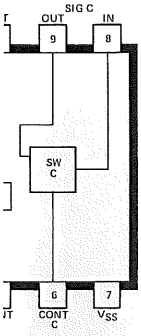
1820-0692





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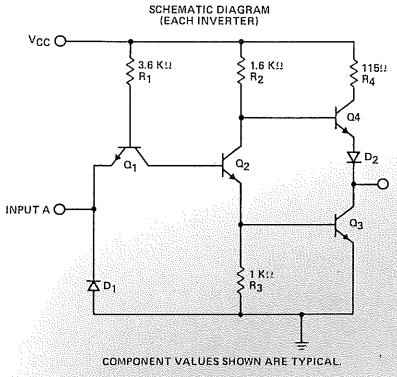

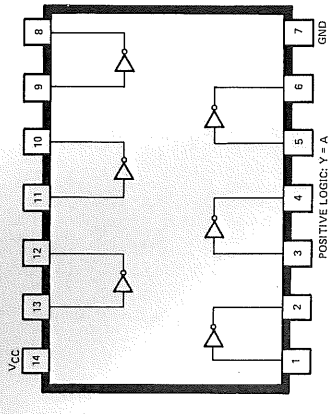

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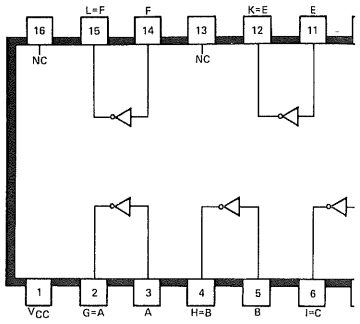

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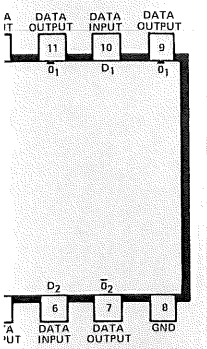

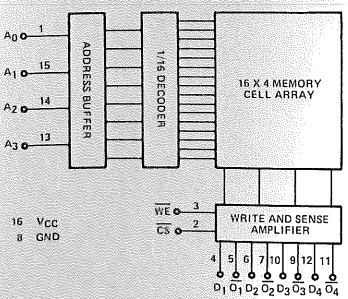

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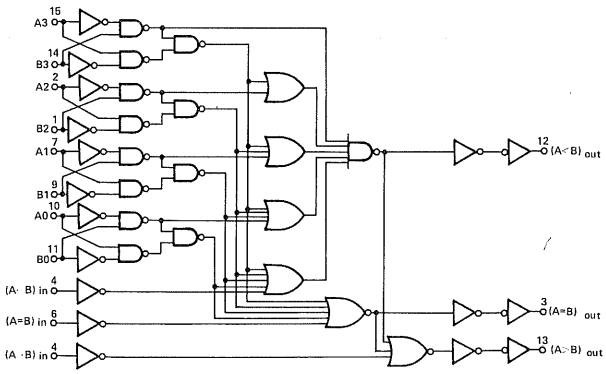

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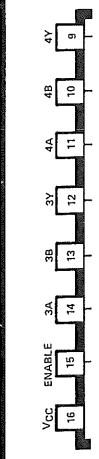
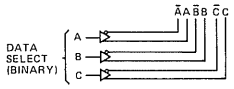
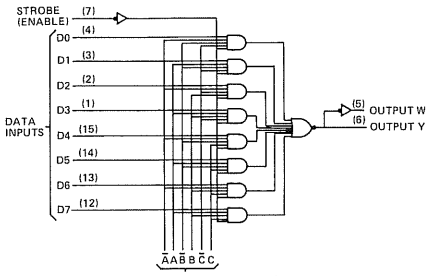


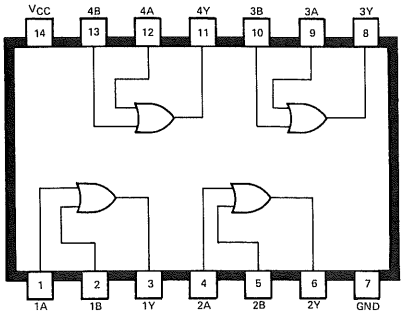
FUNCTION TABLE

INPUTS			OUTPUTS	
SELECT		STROBE		
B	A	S	Y	W
X	X	H	L	H
L	L	L	D0	D0
L	H	L	D1	D1
H	L	L	D2	D2
H	H	L	D3	D3
L	L	L	D4	D4
L	H	L	D5	D5
H	L	L	D6	D6
H	H	L	D7	D7

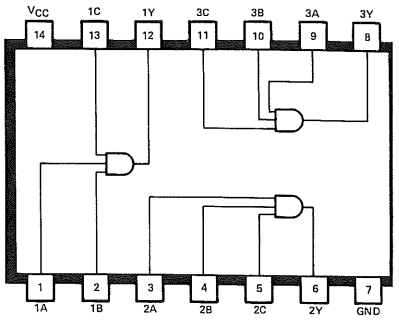




SEE ADDRESS BUFFERS ABOVE



1820-0661



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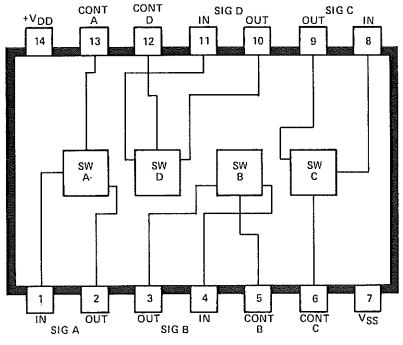
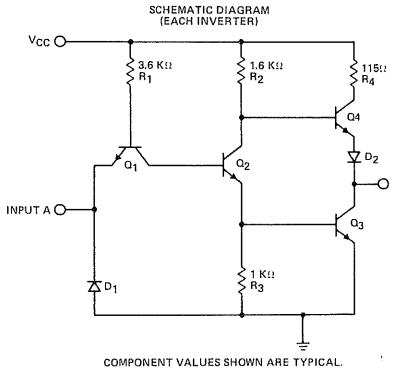


1820-0981



COMPONENT VALUES SHOWN ARE TYPICAL.

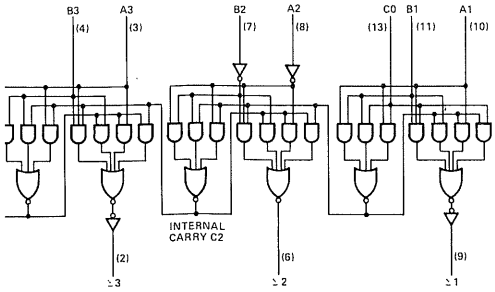
1820-1

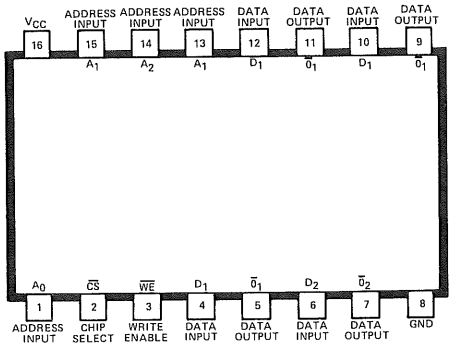
FUNCTION TABLE

INPUT				WHEN CO = L			WHEN CO = H		
				WHEN C2 = L			WHEN C2 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

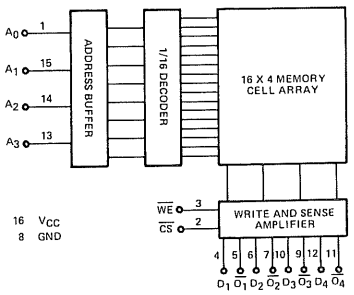
H = HIGH LEVEL, L = LOW LEVEL

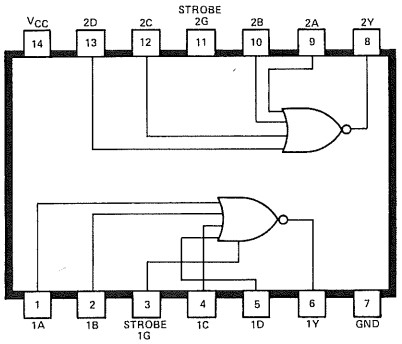
NOTE: INPUT CONDITIONS AT A3, A2, B2, AND C0 ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4 ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.





1820-1106

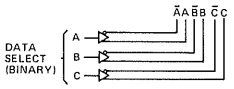


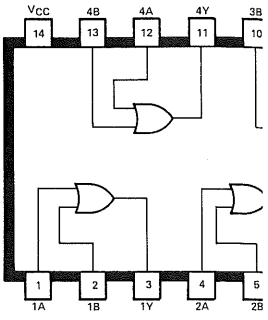


1820-0655

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7





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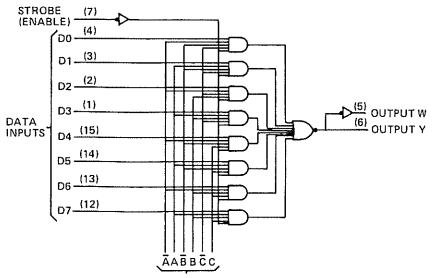
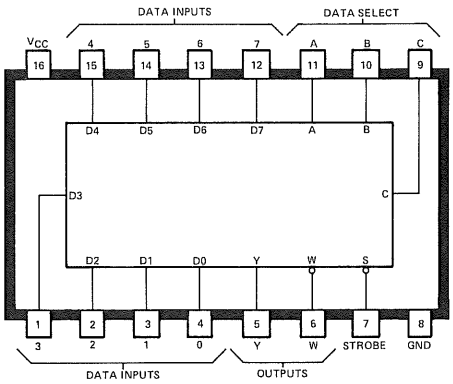
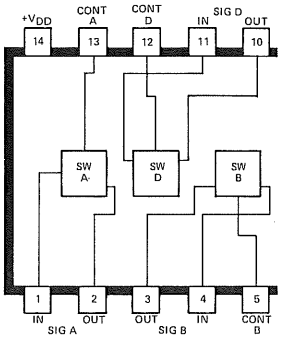


SEE ADDRESS BUFFERS ABOVE

1820-1217





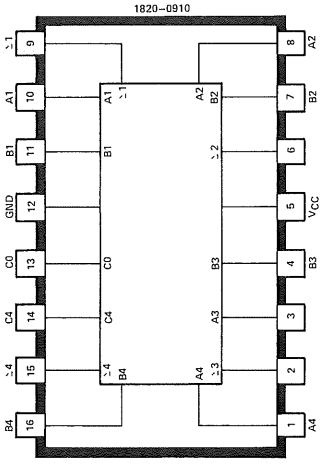
1820-0981

FUNCTION TABLE

INPUT				WHEN CO = L			WHEN CO = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH LEVEL, L = LOW LEVEL

NOTE: INPUT CONDITIONS AT A3, A2, B2, AND C0 ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4 ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.



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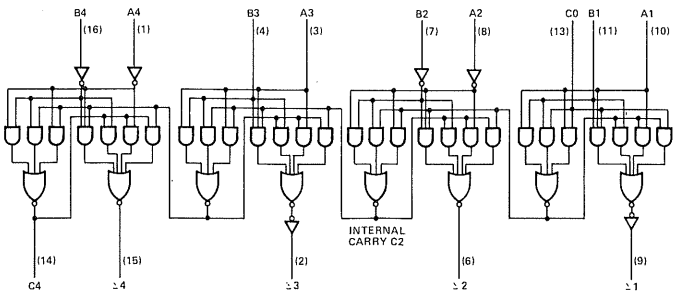

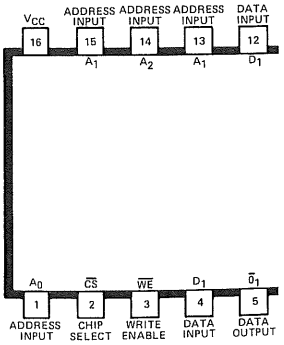

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Oklahoma City 73132
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Tualatin 97062
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TWX: 910-467-8714

PENNSYLVANIA
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Pittsburgh 15238
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Night: 782-0401
TWX: 710-795-3124

1021 8th Avenue
King of Prussia Industrial Park
King of Prussia 19406
Tel: (215) 265-7000
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San Antonio 78226
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TWX: 910-871-1170

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Medical Only
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No. 7 Koger Exec. Center
Suite 212
Norfolk 23502
Tel: (804) 497-1026/7

P.O. Box 9854
2914 Hungary Springs Road
Richmond 23228
Tel: (804) 285-3431
TWX: 710-956-0157

WASHINGTON
Bellefield Office Pk.
1203-114th SE
Bellevue 98004
Tel: (206) 454-3971
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Charleston
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Hewlett-Packard (Canada) Ltd.
11748 Kingsway Ave.
Edmonton T5G 0X5
Tel: (403) 452-3670
TWX: 610-831-2431

Hewlett-Packard (Canada) Ltd.
915-42 Avenue S.E. Suite 102
Calgary T2G 1Z1
Tel: (403) 287-1672

BRITISH COLUMBIA
Hewlett-Packard (Canada) Ltd.
837 E. Cordova Street
Vancouver V6A 3R2
Tel: (604) 254-0531
TWX: 610-922-5059

MANITOBA
Hewlett-Packard (Canada) Ltd.
513 Century St.
St. James
Winnipeg R3H 0L8
Tel: (204) 786-7581
TWX: 610-671-3531

NOVA SCOTIA
Hewlett-Packard (Canada) Ltd.
800 Windmill Road
Dartmouth B3B 1L1
Tel: (902) 469-7820

ONTARIO
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Ottawa K2C 0P9
Tel: (613) 225-6530
TWX: 610-562-8968

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
Mississauga L4V 1L9
Tel: (416) 678-9430
TWX: 610-492-4246

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Hewlett-Packard (Canada) Ltd.
275 Hymus Blvd.
Pointe Claire H9R 1G7
Tel: (514) 697-4232
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TLX: 05-821521 HPCL

Hewlett-Packard (Canada) Ltd.
2376 Galvani Street
Ste-Foy G1N 4G4
Tel: (418) 688-8710

FOR CANADIAN AREAS NOT LISTED:
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CENTRAL AND SOUTH AMERICA

ARGENTINA
Hewlett-Packard Argentina S.A.C.e.I
Lavalle 1171-3° Piso
Buenos Aires
Tel: 35-0436, 35-0627, 35-0341
Telex: 012-1009
Cable: HEWPACK ARG

BOLIVIA
Stambuk & Mark (Bolivia) Ltda.
Av. Mariscal, Santa Cruz 1342
La Paz
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Telex: 3560014
Cable: BUKMAR

BRAZIL
Hewlett-Packard Do Brasil I.E.C. Ltda.
Rua Frei Caneca, 1.152-Bela Vista
01307-**São Paulo**-SP
Tel: 288-71-11, 287-81-20, 287-61-93
Telex: 309151/2/3
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Hewlett-Packard Do Brasil I.E.C. Ltda.
Rua Siqueira Campos, 53, 4° andar Copacabana
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Telex: 2100 79 HEWPACK
Cable: HEWPACK
Rio de Janeiro

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Calcagni y Metcalfe Ltda.
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Casilla 2118
Santiago, 1
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Cable: CALMET

COLOMBIA
Instrumentación
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Apartado Aéreo 6287
Bogota, 1 D.E.
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COSTA RICA
Cientifica Costarricense S.A.
Apartado 10159
San José
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GUATEMALA
IPESA
Avenida La Reforma 3-48, Zona 9
Guatemala
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Hewlett-Packard Mexicana, S.A. de C.V.
Torres Adalid No. 21, 11° Piso
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Ponce de León 154
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Telex: SATRON 3450 332

URUGUAY
Pablo Ferrando S.A.
Comercial e Industrial
Avenida Italia 2877
Casilla de Correo 370
Montevideo
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Apartado 50933
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Handelska 52/3
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DENMARK
Hewlett-Packard A/S
Datavej 52
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DK-8600 **Silkeborg**
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FINLAND
Hewlett-Packard Oy
Nahkahousuntie 5
P.O. Box 6
SF-00211 **Helsinki** 21
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FRANCE
Hewlett-Packard France
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Boite Postale No. 6
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Avenue de Col-Vert, 1,
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Enighetsvägen 1-3
Fack
S-161 20 **Bromma** 20
Tel: (08) 730 05 50
Cable: MEASUREMENTS
Stockholm
Telex: 10721

Hewlett-Packard Sverige AB
Hagakersgatan 9C
S-431 41 **Mölndal**
Tel: (031) 27 68 00/01
Telex: Via Bromma

SWITZERLAND
Hewlett-Packard (Schweiz) AG
Zücherstrasse 20
P.O. Box 64
CH-8952 Schlieren **Zurich**
Tel: (01) 98 18 21
Cable: HPAG CH
Telex: 53933 hpag

Hewlett-Packard (Schweiz) AG
9, chemin Louis-Pictet
*CH-1214 Vernier-***Geneva**
Tel: (022) 41 49 50
Cable: HEWPACKSA Geneva
Telex: 27 333 hpsa ch

TURKEY
Telekom Engineering Bureau
Saglik Sok No. 15/1
Ayaspasa-Beyoglu
P.O. Box 437 Beyoglu
TR-**Istanbul**
Tel: 49 40 40
Cable: TELEMATION Istanbul

UNITED KINGDOM
Hewlett-Packard Ltd.
King Street Lane
Winnersh, Wokingham
GB-**Berkshire** RG11 5AR
Tel: Wokingham 784774
Telex: 847178/848179

Hewlett-Packard Ltd.
"The Graftons"
Stamford New Road
GB-**Altrincham**, Cheshire
Tel: (061) 928-9021
Telex: 668068

Hewlett-Packard Ltd.
c/o Makro
South Service Wholesale Centre
Amber Way
Halesowen Industrial Estate
GB-**Halesowen**, Worcs
Tel: Birmingham 7860

Hewlett-Packard Ltd.
4th Floor
Wedge House
799, London Road
GB-**Thornton Heath** CR4 6XL.
Surrey
Tel: (01) 684 0105
Telex: 946825

Hewlett-Packard Ltd.
c/o Makro
South Service Wholesale Centre
Wear Industrial Estate
Washington
GB-**New Town**, County Durham
Tel: Washington 464001 ext. 57/58

Hewlett-Packard Ltd.'s registered address for V.A.T. purposes only:
70, Finsbury Pavement
London, EC2A1SX
Registered No. 690597

USSR
Hewlett-Packard USSR
c/o Commercial Office
American Embassy (Box M)
A-1091 **Vienna**, Austria
Tel: 221-79-71
Telex: 7825 hewpak SU

YUGOSLAVIA
Iskra-Standard/Hewlett-Packard
Office
Miklosiceva 38/VII
61000 **Ljubljana**
Tel: 315-879/321-674
Telex: 31265

SOCIALIST COUNTRIES PLEASE CONTACT:
Hewlett-Packard S.A.
7, rue du Bois-du-Lan
P.O. Box 349
CH-1217 Meyrin 1 **Geneva**
Switzerland
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 2 24 86

AFRICA, ASIA, AUSTRALIA

ANGOLA
Telectra
Empresa Técnica de
Equipamentos
Eléctricos, S.A.R.L.
R. Barbosa Rodrigues, 42-1°D1.°
Caixa Postal, 6487-**Luanda**
Tel: 35515/6
Cable: TELECTRA Luanda

AUSTRALIA
Hewlett-Packard Australia
Pty. Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Tel: 89-6351, 89-6306
Telex: 31-024
Cable: HEWPARD Melbourne

Hewlett-Packard Australia
Pty. Ltd.
31 Bridge Street
Pymble,
New South Wales, 2073
Tel: 449-6566
Telex: 21561
Cable: HEWPARD Sydney

Hewlett-Packard Australia
Pty. Ltd.
97 Churchill Road
Prospect 5082
South Australia
Tel: 44 8151
Cable: **HEWPARD** Adelaide

Hewlett-Packard Australia
Pty. Ltd.
141 Stirling Highway
Claremont, W.A. 6010
Tel: 86-5455
Telex: 93859
Cable: HEWPARD

Hewlett-Packard Australia
Pty. Ltd.
121 Wollongong Street
Fyshwick, A.C.T., 2609
Tel: 95 3733

Hewlett-Packard Australia
Pty. Ltd.
5th Floor
Teachers Union Building
495-499 Boundary Street
***Spring Hill**, 4000 Queensland*
Tel: 29-1544
Telex: AA-42133

CEYLON
United Electricals Ltd.
P.O. Box 681
60, Park St.
Colombo 2
Tel: 26696
Cable: HOTPOINT Colombo

CYPRUS
Kypronics
19 Gregorios & Xenopoulos Rd.
P.O. Box 1152
CY-**Nicosia**
Tel: 45628/29
Cable: KYPRONICS PANDEHIS

HONG KONG
Schmidt & Co.(Hong Kong) Ltd.
P.O. Box 297
Connalight Centre
39th Floor
Connaught Road, *Central*
Hong Kong
Tel: 255291
Telex: 74766SCHMCHX
Cable: SCHMIDTCO Hong Kong

INDIA
Blue Star Ltd.
Kasturi Buildings
Jamshedji Tata Rd.
Bombay 400 020
Tel: 29 50 21
Telex: 3751
Cable: BLUEFROST

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
Bombay 400 025
Tel: 45 78 87
Telex: 4093
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Blue Star Ltd.
Band Box House
Prabhadevi
Bombay 400 025
Tel: 45 73 01
Telex: 3751
Cable: BLUESTAR

Blue Star Ltd.
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Kanpur 208 001
Tel: 6 88 82
Cable: BLUESTAR

Blue Star Ltd.
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Telex: 459

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Cable: MULTICORP Tehran
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1-59-1 Yoyogi
Shibuya-ku, **Tokyo**
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Cable: YHPMARKET TOK 23-724

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Osaka
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Nakamura-ku, **Nagoya** City
Tel: (052) 571-5171

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Tel: 27091, 27114
Telex: 6-203 Negon Mo
Cable: NEGON

NEW ZEALAND
Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
Kilbirnie, Wellington 3
Mailing Address:
Hewlett-Packard (N.Z.) Ltd.
P.O. Box 9443
Courtney Place
Wellington
Tel: 877-199
Telex: NZ 3898

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Box 51092
Pakuranga
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tions Ltd. *(TEIL)*
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Cable: COOPERATOR Karachi

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Tel: 41924
Cable: FEMUS Rawalpindi

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Makati, Rizal
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Tel: 633022
Telex: HPSG RS 21486
Cable: HEWPACK, Singapore

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Sandton, Transvaal 2001
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Bree Street
Cape Town
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Cable: HEWPACK Cape Town
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Telex: 6-7954

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BP 1741
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EWLETT PACKARD

SIX BIT DATA PROBE

MODEL 10231B

OPERATING NOTE/AUGUST 1974

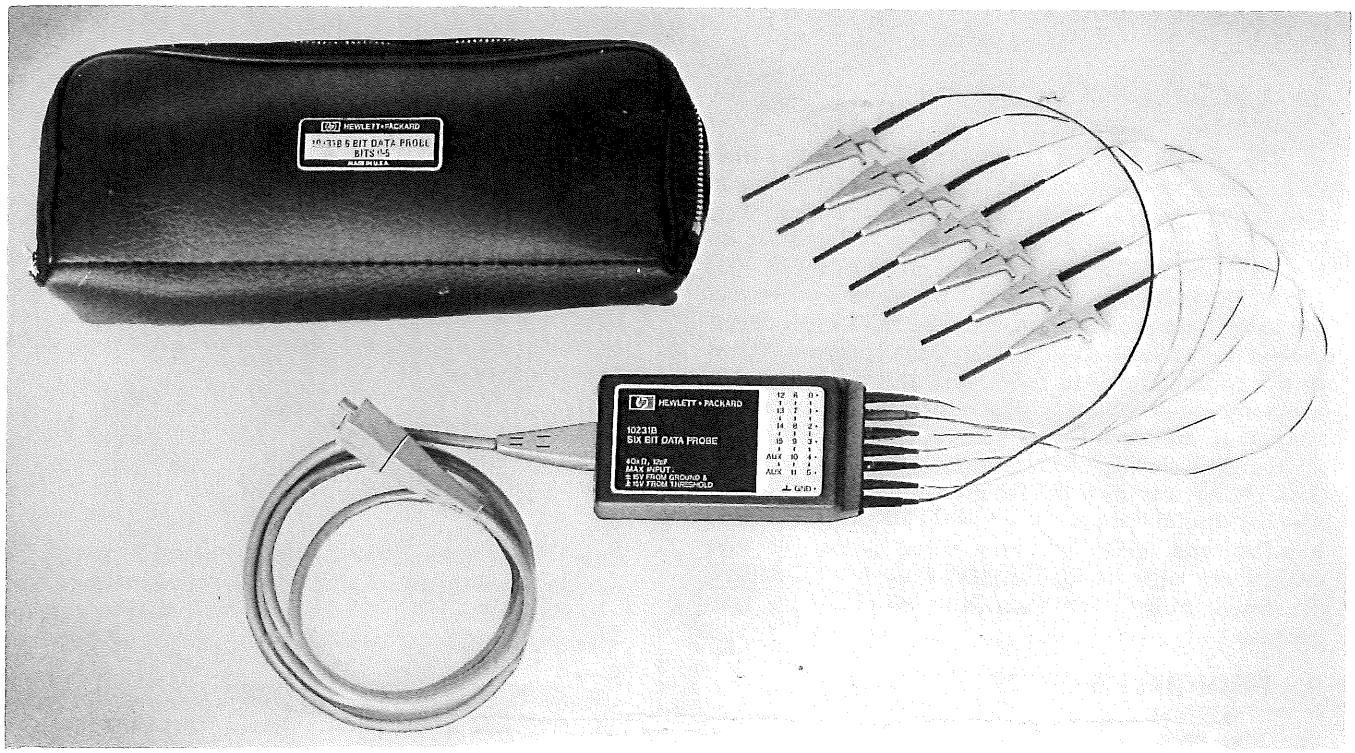

Figure 1. Model 10231B Six Bit Data Probe

1. INTRODUCTION.

2. This operating note provides operating and service information for the Hewlett-Packard Model 10231B Six Bit Data Probe (figure 1).

3. DESCRIPTION.

4. The Model 10231B is an active probe providing six channels of TTL (transistor-transistor logic) digital data to a Logic Analyzer (i.e., Hewlett-Packard Model 1601A Logic State Analyzer or Hewlett-Packard Model 1620A Pattern Analyzer) without significant loading of the circuitry under test. Minimal loading is maintained by placing active circuitry in a compact pod located near the point of test. Signal shaping and amplification is accomplished by comparators in series with each input. Probe operating power is supplied by the logic analyzer through the interconnecting cable. The Model 10231B connects to a logic-analyzer front panel by means of a 17-pin miniature snap-in connector. Refer to table 1 for complete specifications and instrument compatibility for the Model 10231B.

Table 1. Specifications

PROBE INPUTS
INPUT RC: 40 ±3KΩ shunted by ≤14 pF. INPUT BIAS CURRENT: ≤20 μA. INPUT THRESHOLD: TTL, fixed at +1.45 ±0.05 Vdc. Variable to ±10 Vdc. MINIMUM INPUT SWING: 0.5V p-p ±5% of threshold voltage. MAXIMUM INPUT: Level, ±15 Vdc max. Swing, 15V peak from threshold.
INSTRUMENT COMPATIBILITY
HP Model 1601A, Logic State Analyzer. HP Model 1620A, Pattern Analyzer.

5. CLAIMS.

6. Upon receipt, inspect the instrument for damage and if none is noted, accomplish the performance

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For more information, call the local HP Sales Office or East (201) 265-5000 . Midwest (312) 677-0400 . South (404) 436-6181 West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Cable "HEWPACKSA" Tel (022) 41.54.00 or write Hewlett-Packard, 1217 Meyrin-Geneva, Switzerland.

checks. Hewlett-Packard Company guarantees the performance of the instrument as stated in the certification located near the back of this note. If the physical or operating conditions of the instrument are unsatisfactory, notify the carrier and the nearest HP Sales/Service Office immediately. HP will arrange for repair or replacement without waiting for settlement of the claim by the carrier.

7. ACCESSORIES.

8. The Model 10231B is supplied with six 12-inch color coded connection leads, six detachable hook-type circuit probes, ground lead and a vinyl carrying case. Each connecting lead has a 6 x 32 screw tip on the end which attaches to the comparator pod, and a 0.025-inch female square-pin tip on the other end for backplane pin connections. The hook-type circuit probes have recessed male pins which can be attached to the connecting lead ends. The ground lead has a nondetachable alligator clip which will support the weight of the circuit pod. In addition, labels designating Bit 6 through Bit 11, and Bit 12 through Bit 15, SER QUAL and SER DATA are supplied for use with two additional data probes. Vinyl carrying cases with handles and space to carry three probes or four probes are also available (HP Part No. 1540-0250 for three probes, HP Part No. 1540-0325 for four probes).

9. PRINCIPLES OF OPERATION.

10. The Model 10231B circuitry consists of a —6.2-volt supply, six identical comparators, and six inverting line drivers which buffer, amplify, and convert input data to a TTL compatible output (see figure 3).

11. The —6.2-volt supply consists of R19, VR1, C17, C18, C19. R19 and VR1 form a voltage divider and regulator which reduces the —12-volt input to —6.2 volts. C17, C18 and C19 bypass line variations to ground.

12. The Model 10231B accepts positive or negative input data up to 15 volts peak in amplitude with threshold levels up to ±10Vdc.

13. U8 and U9 are resistor networks which form voltage dividers at the data inputs to each comparator. The 26.1 kilohm and 13 kilohm resistors form voltage dividers which scale input data voltage swings to levels compatible with the comparator inputs. The reference threshold voltage supplied by the Logic Analyzer has also been scaled by a factor of three. For example, the threshold for transistor-transistor logic is typically +1.5 Vdc. The reference TTL threshold supplied by the Logic Analyzer is approximately +0.5 Vdc. The 8.68 kilohm resistor on the threshold input line matches the threshold input impedance of the comparator to the data input impedance.

14. In the static condition, the outputs of comparators U1 through U6 are LO (approximately +0.5 Vdc). When the input data voltage level exceeds the threshold level, the output will go HI (approximately +3V). The comparator outputs are inverted by U7A through U7F and applied to the logic analyzer.

15. Each comparator has positive feedback through two 1-megohm resistors which form a hysteresis band preventing comparator oscillation if the data input voltage level occurs at the exact threshold of the comparator.

16. MAINTENANCE.

17. PERFORMANCE TESTS.

18. The Model 10231B must be tested as part of the logic analyzer that the probe is supplied with. Refer to the following performance tests in Section V of the logic analyzer operating and service manual.

Input Threshold	Input RC
Input Logic Swing	Input Bias Current

19. REPAIR.

20. When repairing A1, be careful to prevent breakage of small wires where W1 is soldered to A1.

21. REPLACEABLE PARTS.

22. Table 2 lists the replaceable parts and identifies the Hewlett-Packard part number of each item. Figure 2 shows the location of each component. Figure 4 is an exploded view of the Model 10231B.

23. To order a replaceable part from Hewlett-Packard, address the order to the nearest HP Sales/Service Office. Include the probe model number, the serial number, the reference designation of the part, and the HP Part number. If a part is not listed, provide a description of the part, including function and location.

24. Board assembly A1 is not sold separately. To obtain a replacement assembly, the entire probe unit must be ordered. Order HP Model 10231B.

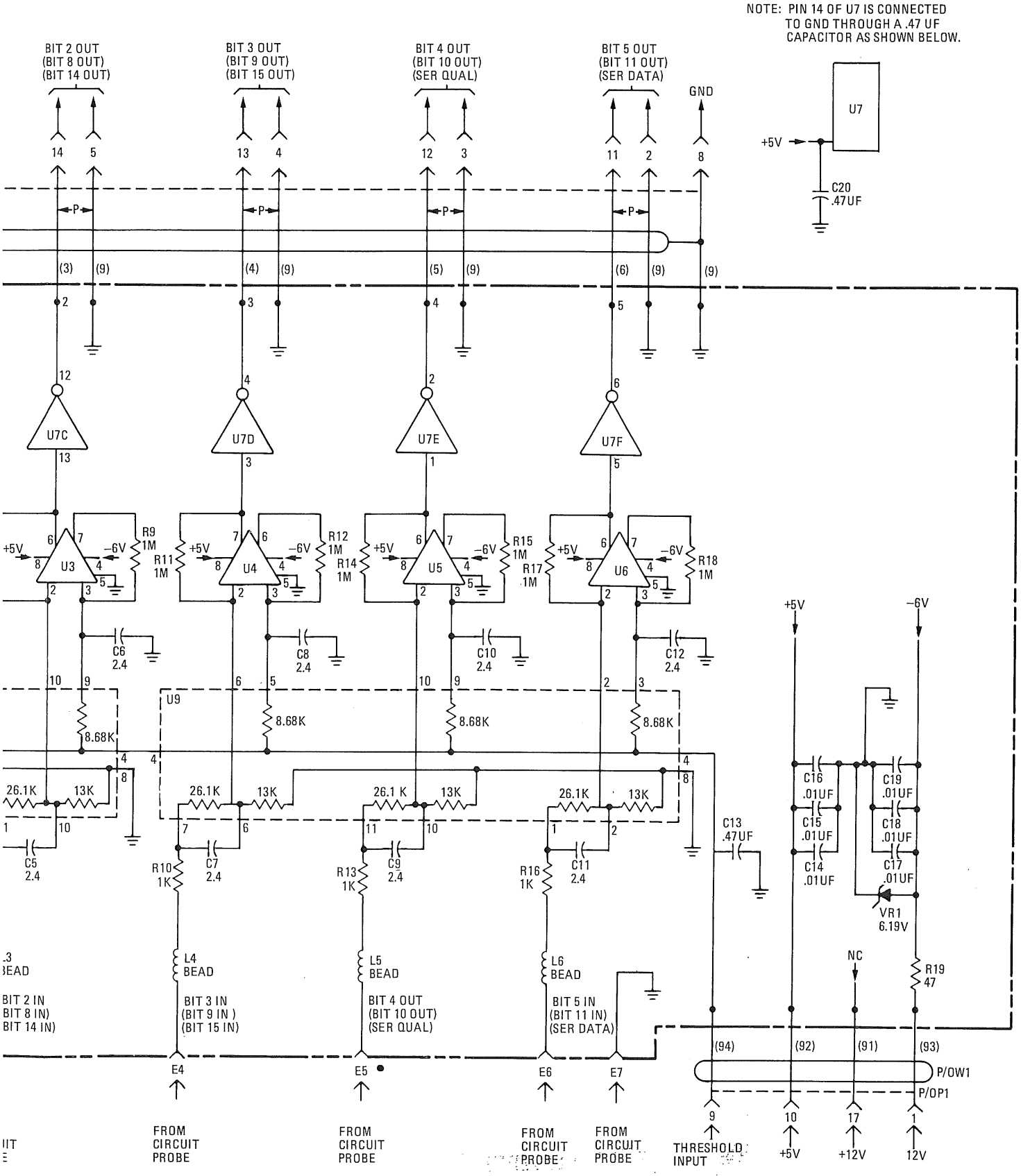
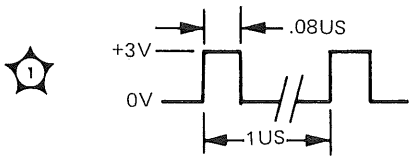
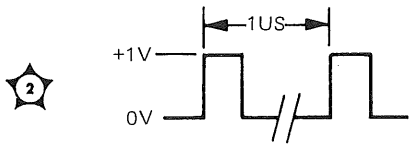
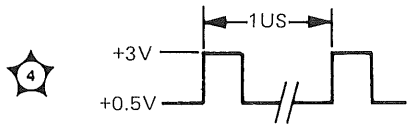
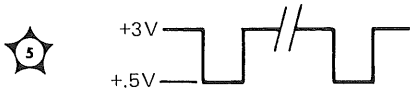


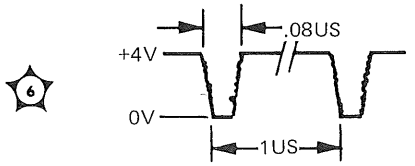
Figure 3.
Model 10231B Schematic
Page 3



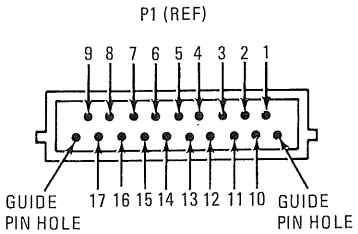


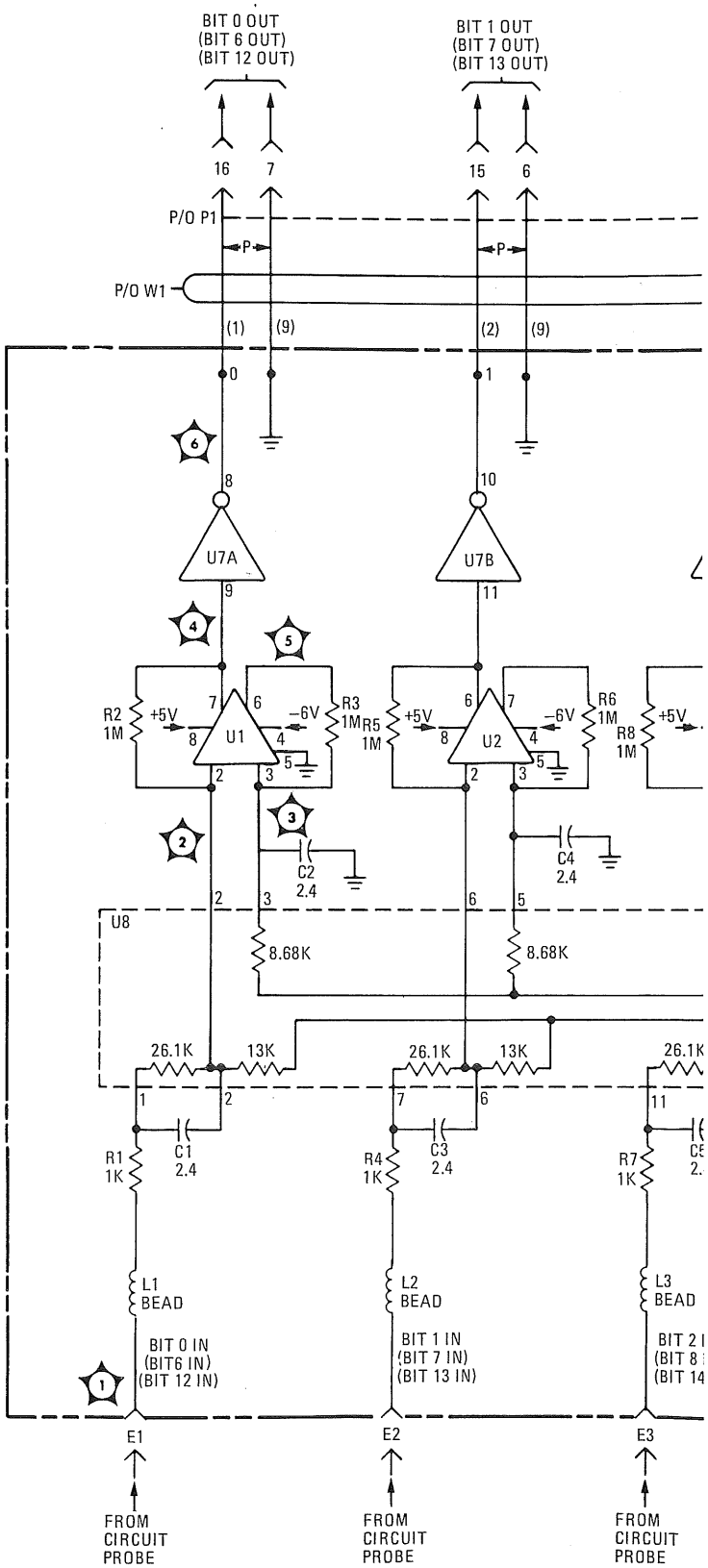


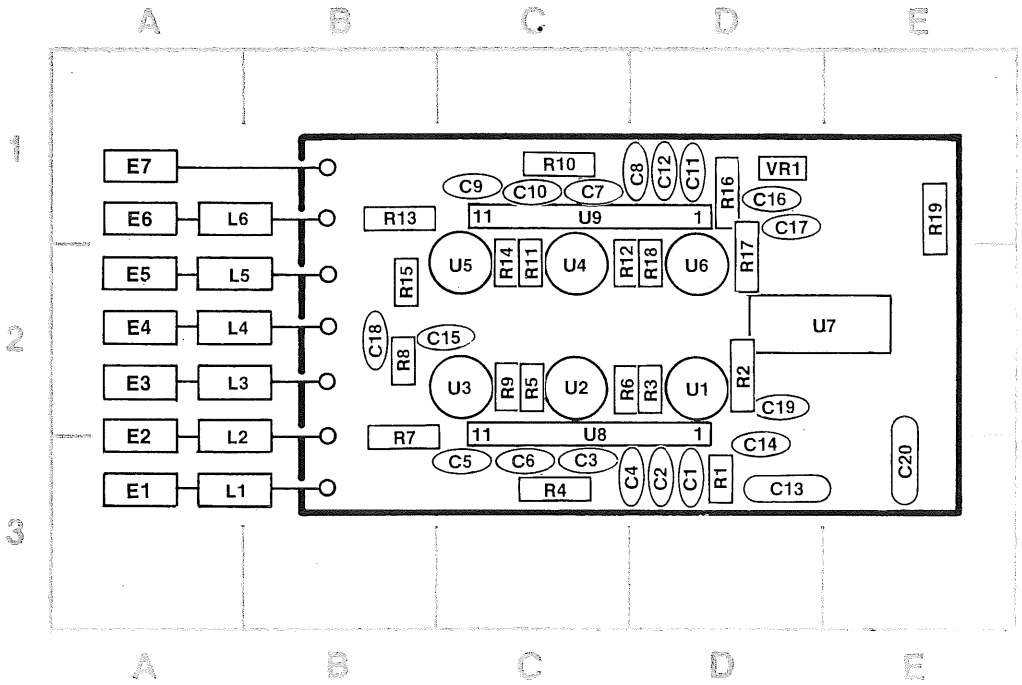




NOTE: NUMBERS IN PARENTHESES (1) INDICATE WIRE COLOR USING RESISTOR WIRE COLOR CODE.







REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-3	L5	A-2
C2	D-3	L6	A-1
C3	C-3	R1	D-3
C4	D-3	R2	D-2
C5	C-3	R3	D-2
C6	C-3	R4	C-3
C7	C-1	R5	C-2
C8	D-1	R6	C-2
C9	C-1	R7	B-2
C10	C-1	R8	B-2
C11	D-1	R9	C-2
C12	D-1	R10	C-1
C13	D-3	R11	C-2
C14	D-3	R12	C-2
C15	C-2	R13	B-1
C16	D-1	R14	C-2
C17	D-1	R15	B-2
C18	B-2	R16	D-1
C19	D-2	R17	D-2
C20	E-3	R18	D-2
E1	A-3	R19	E-1
E2	A-3	U1	D-2
E3	A-2	U2	C-2
E4	A-2	U3	C-2
E5	A-2	U4	C-2
E6	A-1	U5	C-2
E7	A-1	U6	D-2
L1	A-3	U7	E-2
L2	A-3	U8	C-2
L3	A-2	U9	C-1
L4	A-2	VR1	D-1

Figure 2. Model 10231B Component Identification

Table 2. Replaceable Parts (Cont'd)

Reference Designation	HP Part No.	Qty	Description	Mfr. Code	Mfr. Part No.
A1R7	0675-1021		R: Fxd 1 K 10% .125 W CC Tubular	01121	BB 1021
A1R8	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R9	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R10	0675-1021		R: Fxd 1K 10% .125 W CC Tubular	01121	BB 1021
A1R11	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R12	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R13	0675-1021		R: Fxd 1 K 10% .125 W CC Tubular	01121	BB 1021
A1R14	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R15	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R16	0675-1021		R: Fxd 1 K 10% .125 W CC Tubular	01121	BB 1021
A1R17	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R18	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R19	0698-3698	1	R: Fxd 47 5% 1W Mo Tubular	16299	FP32-1-T0047R0-J
A1U1 Thru A1U6	1826-0236	6	IC: DGTL, Comparator	18324	UA760
A1U7	1820-0683	1	IC: DGTL, Inverter	01295	SN74S04N
A1U8	1810-0211	2	CIRCUIT: PSIV, Non-Rprable In	28480	1810-0211
A1U9	1810-0211		CIRCUIT: PSIV, Non-Rprable In	28480	1810-0211
A1VR1	1902-0551	1	DIODE: Zener 6.19 V VZ, 1W Max Pd	04713	SZ 11213-80

Table 2. Replaceable Parts

Reference Designation	HP Part No.	Qty	Description	Mfr. Code	Mfr. Part No.
CP1 Thru CP6	10230-62101	7	PROBE ASSY: Circuit	28480	10230-62101
MP1	5040-7683	1	COVER: Top	28480	5040-7683
MP2	5040-7685	1	COVER: Bottom	28480	5040-7685
MP3	7120-4389	1	LABEL: Ident	28480	7120-4389
MP4	7120-4383	1	LABEL SET: Ident, Orange	28480	7120-4383
MP5	7120-4388	1	LABEL SET: Ident, Green	28480	7120-4388
MP6	1540-0251	1	CASE: Carrying	28480	1540-0251
W1	10231-61601	1	CABLE ASSY: 17 Pin	28480	10231-61601
W2	10231-61608	1	CABLE: Pin Adapter; White/Black	28480	10231-61608
W3	10231-61612	1	CABLE: Pin Adapter; White/Brown	28480	10231-61612
W4	10231-61613	1	CABLE: Pin Adapter; White/Red	28480	10231-61613
W5	10231-61614	1	CABLE: Pin Adapter; White/Orange	28480	10231-61614
W6	10231-61615	1	CABLE: Pin Adapter; White/Yellow	28480	10231-61615
W7	10231-61616	1	CABLE: Pin Adapter; White/Green	28480	10231-61616
W8	10231-61611		CABLE: Ground	28480	10231-61611
A1C1 Thru A1C12	0160-3592	12	C: Fxd Cer 2.4 pF ±.5 pF 200 Vdcw	28480	0160-3592
A1C13	0160-0174	2	C: Fxd Cer 0.47 μF +0 —20% 25 Vdcw	56289	5C1187S-CML
A1C14 Thru A1C19	0160-3451	6	C: Fxd Cer 0.47 μF +80 —20% 100 Vdcw	56289	C0238101F103ZS25-CD
A1C20	0160-0174		C: Fxd Cer 0.01 μF +80 —20% 25 Vdcw	56289	561187S-CML
A1E1 Thru A1E6	10230-25701	6	NUT: Cable Connector	28480	10230-25701
A1E7	10230-25702	1	INSERT: Threaded	28480	10230-25702
A1L1 Thru A1L6	9170-0029	6	CORE: Ferrite Bead	02114	56-590-65A2/4A
A1R1	0675-1021	6	R: Fxd 1 K 10% .125 W CC Tubular	01121	BB 1021
A1R2	0698-4073	12	R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R3	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R4	0675-1021		R: Fxd 1 K 10% .125 W CC Tubular	01121	BB 1021
A1R5	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051
A1R6	0698-4073		R: Fxd 1 M 10% .125 W CC Tubular	01121	BB 1051

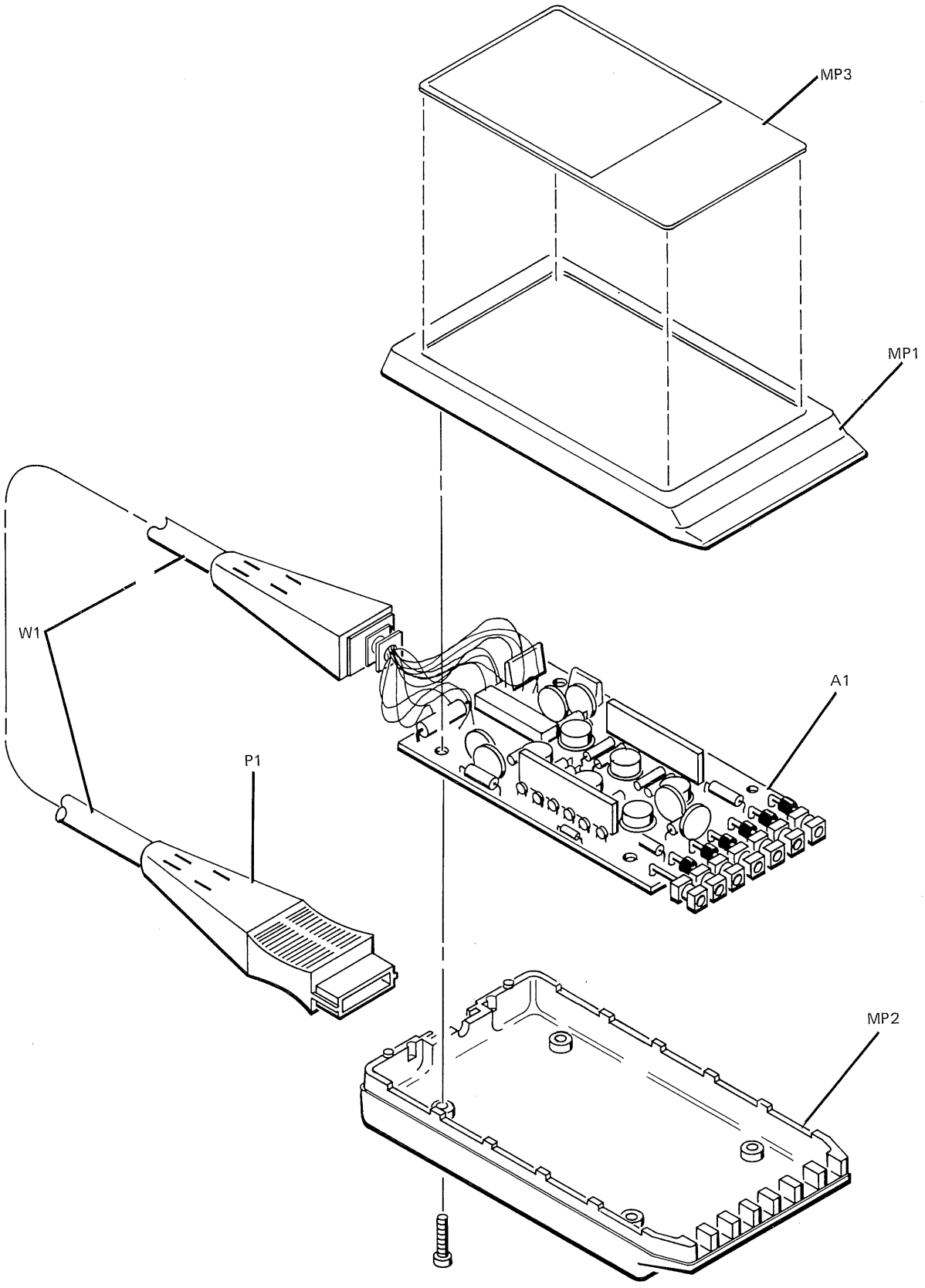


Figure 4. Model 10231B Exploded View

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

Service contracts or customer assistance agreements are available for Hewlett-Packard products that require maintenance and repair on-site.

C W&A 6/74

MANUAL CHANGES

MODEL 1600A
LOGIC STATE ANALYZER

Manual Serials Prefixed: 1533A
Manual Printed: SEPT 1975

Make all changes listed below as Errata. Check the following table for your instrument serial prefix and/or serial number and make listed change(s) to the manual:

Serial Prefix or Number	Make Changes	Serial Prefix or Number	Make Changes

Δ ERRATA

Page 5-4, paragraph 5-14,
Step e: Revise CLOCK setting i.e., neg. slope.
Delete: Step k.
Page 5-4, figure 5-4,
Show all data probes and the clock probe connected directly to the function generator.
Show monitor oscilloscope connected to function generator through a 10:1 probe.
Page 5-7, paragraph 5-18,
50Ω ±2Ω: Change to read 50Ω ±2.5Ω in step b.
Page 5-9, figure 5-10,
(LWE WIDTH): Change to read (HDL TRAILING EDGE).
(HDL TRAILING EDGE): Change to read (LWE WIDTH).
Page 5-10, paragraph 5-24,
A1C37: Change to read A1C41 in step k.
A1C41: Change to A1C37 in step l.
Page 6-3, figure 6-1,
Add: MP58 to component shown below MP7.
Add: MP59, screw, to hold on top and bottom instrument covers.
Add: MP60 to screw holding pouch on top cover.
Page 6-4, figure 6-1,
Add: MP57, shield, sheet metal, attaching to MP38 and shields T1.
Table 6-2,
F1: Add to description STANDARD.
Add: F1, HP Part No. 2110-0016, FUSE 0.6A 250V SLO-BLO (OPTIONS 900-902, 906), Mfr Code 71400, Mfr Part No. MDL-6/10.
J4: Change to HP Part No. 1250-0659, CONNECTOR-RF TPS FEM SGL-HOLE-FR 50-OHM, Mfr Code 24931, Mfr Part No. 23JR107-1.

Table 6-2 (Cont'd),
J6: Add to description PART OF W5.
MP31: Add to description PART OF W6.
Delete: MP32.
MP33: Change HP Part No. and Mfr Part No. to 01600-24701.
MP47: Change HP Part No. and Mfr Part No. to 01600-60602.
MP54: Change HP Part No. and Mfr Part No. to 175A-91.
Add: MP57, HP Part No. 01600-00601, SHIELD:TRANSFORMER, Mfr Code 28480, Mfr Part No. 01600-00601.
Add: MP58, HP Part No. 01600-01206, BRACKET:PC HOLDON, Mfr Code 28480, Mfr Part No. 01600-01206.
Add: MP59, HP Part No. 2200-0762, SCREW, MACH 4-40 BLACK, Mfr Code 28480, Mfr Part No. 2200-0762.
Add: MP60, HP Part No. 2360-0197, SCREW, 6-32 X .375, Mfr Code 28480, Mfr Part No. 2360-0197.
Add: Q3, HP Part No. 1854-0433, TRANSISTOR NPN SI PD=90W FT=2MHZ, Mfr Code 28480, Mfr Part No. 1854-0433.
Add: W17 HP Part No. 01600-61602, CABLE, POWER LIGHT AND THRESHOLD SWITCH, Mfr Code 28480, Mfr Part No. 01600-61602.
XV1: Add to Description PART OF W6.
A1C53: Change to HP Part No. 0160-3447, CAPACITOR-FXD 470 PF +—10% 1000WVDC, Mfr Code 28480, Mfr Part No. 0160-3447.
A1J1: Delete HP and Mfr Part No. Change description to CONSISTS OF A1J1E1, A1J1MP1, AND A1J1MP2.
Add: A1J1E1, HP Part No. 1251-0699, CONNECTOR: MALE 17-PIN, Mfr Code 4H713, Mfr Part No. 280-50-00-002.
Add: A1J1MP1, HP Part No. 5040-7478, HOUSING:TOP CONNECTOR, Mfr Code 28480, Mfr Part No. 5040-7478.

June 14 1976
Δ = Latest additions to this change sheet.
This change sheet supersedes all prior change sheets for this manual.

Supplement A for
01600-90903

Δ ERRATA (CONT'D)

Table 6-2 (Cont'd),

Add: A1J1MP2, HP Part No. 5040-7479, HOUSING: BOTTOM CONNECTOR, Mfr Code 28480, Mfr Part No. 5040-7479.

A1J2: Delete HP and Mfr Part Nos. Change description to CONSISTS OF A1J1E1, A1J1MP1, AND A1J1MP2.

A1J3: Delete HP and Mfr Part Nos. Change description to CONSISTS OF A1J1E1, A1J1MP1, AND A1J1MP2.

A1J4: Delete HP and Mfr Part Nos. Change description to CONSISTS OF A1J1E1, A1J1MP1, AND A1J1MP2.

A1J5 through A1J9: Change to HP Part No. 1200-0474, SOCKET, ELECT, IC 14-CONT DIP SLDR TERM, Mfr Code 06776, Mfr Part No. ICN-143-S3.

Delete: A1MP1 and A1MP2.

A1R28: Change to HP Part No. 0757-0401, RESISTOR 100 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-101-F.

A1R29: Change to HP Part No. 0757-0407, RESISTOR, 200 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-201-F.

A1R77: Change to HP Part No. 0684-4711, RESISTOR 470 10% .25W CC, Mfr Code 01121, Mfr Part No. CB4711.

Add: A1R78, HP Part No. 0757-0457, RESISTOR 47.5K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-4752-F.

A2R20: Change to HP Part No. 0684-4711, RESISTOR 470 10% .25W CC TC=0+529, Mfr Code 01121, Mfr Part No. CB4711.

A3C1: Change to HP Part No. 0180-0484, CAPACITOR-FXD; 250 UF +50−10% 200VDC AL, Mfr Code 56289, Mfr Part No. 36D251F200AA2A-DQB.

A3C5: Change to HP Part No. 0180-0484, CAPACITOR-FXD 4500 UF +75−10% 25VDC AL, Mfr Code 56289, Mfr Part No. 36D452G025AA-2B-DQB.

A3MP4: Add to Description NOT SUPPLIED WITH A3, ORDER SEPARATELY.

Add: A6S1, HP Part No. 3101-0576, SWITCH-TGL SUBMIN SPDT NS 2A 250VAC, Mfr Code 28480, Mfr Part No. 3101-0576.

A7C11: Change to HP Part No. 0140-0231, CAPACITOR-FXD 440 PF +−1% 300WVDC MICA, Mfr Code 72136, Mfr Part No. DM15F441FO300WV1C.

Delete: A7CR3 and A7CR4.

A7Q5: Change to HP Part No. 1854-0071, TRANSISTOR NPN SI PD=300MW FT= 200 MHZ, Mfr Code 28480, Mfr Part No. 1854-0071.

A7Q18: Change to HP Part No. 1854-0071, TRANSISTOR NPN SI PD=300MW FT=200 MHZ, Mfr Code 28480, Mfr Part No. 1854-0071.

A7R1: Change to HP Part No. 0757-0441, RESISTOR 8.25K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-8251-F.

Table 6-2 (Cont'd),

A7R32: Change to HP Part No. 0675-6811, RESISTOR 680 10% .125W CC, Mfr Code 01121, Mfr Part No. BB6811.

A7R33: Change to HP Part No. 0757-0443, RESISTOR 11K 1% .125W F TC=0+−100 Mfr Code 24546, Mfr Part No. C4-1/8-TO-1102-F.

A7R34: Change to HP Part No. 0757-0441, RESISTOR 8.25K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-8251-F.

A7R35: Change to HP Part No. 0684-4731, RESISTOR 47K 10% .25W FC TC=−400/+800, Mfr Code 01121, Mfr Part No. CB4731.

A7R36: Change to HP Part No. 0757-0442, RESISTOR 10K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-1002-F.

A7R61: Change to HP Part No. 0757-0920, RESISTOR 680 2% .125W F TUBULAR, Mfr Code 24546, Mfr Part No. C4-1/8-TO-681-G.

A7R62: Change to HP Part No. 0757-0441, RESISTOR 8.25K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-8251-F.

A7R64: Change to HP Part No. 0684-4731, RESISTOR 47K 10% .25W FC TC=−400/+800, Mfr Code 01121, Mfr Part No. CB4731.

A7R82: Change to HP Part No. 0757-0920, RESISTOR 680 2% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-681-G.

A7R86: Change to H P Part No. 0684-4731, RESISTOR 47K 10% .25W FC TC=−400/+800, Mfr Code 01121, Mfr Part No. CB4731.

A7R87: Change to HP Part No. 0698-7096, RESISTOR 10 10% .125W CC TC=0+588, Mfr Code 01121, Mfr Part No. BB1001.

A7R88: Change to HP Part No. 0698-7096, RESISTOR 10 10% .125W CC TC=0+588, Mfr Code 01121, Mfr Part No. BB1001.

A7R89: Change to HP Part No. 0757-0442, RESISTOR 10K 1% .125W F TC=0+−100, Mfr Code 24546, Mfr Part No. C4-1/8-TO-1002-F.

A7VR2: Change to HP Part No. 1902-3114, DIODE-ZNR 6.19V 5% PD=.4W, Mfr Code 04713, Mfr Part No. SZ10939-123.

A8R48: Change to HP Part No. 0684-1021, RESISTOR IK 10% .25W FC TC=−400/+600, Mfr Code 01121, Mfr Part No. CB1021.

Delete: A8R49.

Add: A8R52, HP Part No. 0684-1011, RESISTOR 100 10% .25W FC TC=−400/+500, Mfr Code 01121, Mfr Part No. CB1011.

Add: A8R53, HP Part No. 0757-0448, RESISTOR 18.2K 1% .125W F, Mfr Code 24546, Mfr Part No. C4-1/8-TO-1822-F.

Δ ERRATA (CONT'D)

Schematic 1,
Add: W17 to designate wires from A1 to R1, DS6, and TP1.
Page 8-10, figure 8-9,
R1: Change reference designator to R2.
R2: Change reference designator to R1.
Schematic 2,
A3R2: Change value to 220K.
A3R6: Change value to 100K.
A3R13: Change value to 1780.
Schematic 3,
R8: Change wire color (8) to read (2).
A2R27: Change +110V connection to +12V.
A2R31: Maintain connection to +110V.
V1: Change wire colors as follows: (945) to read (934), (934) to read (93), 9 to read (5), 8 to read (945).
REAR VIEW NECK PIN CONNECTIONS: Change wire colors as follows: (945) to read (934), and (934) to read (945).
Schematic 4,
A7U22: Show all resistor values as 6000 ohms.
A4U3: Show all resistor values as 6000 ohms.
A5U3: Show all resistor values as 6000 ohms.
Schematic 5,
Add: W17 designation to wires to TP1, R1, R10, and DS6.
Schematic 7,
A1R28: Change value to 100.
A1R29: Change value to 200.
Schematic 9,
A1L22: Change value to 1.5.
Schematic 11,
A1C53: Change value to 470.
Schematic 15,
A8U31A: Pin 5 change number to 4, and pin 4 change number to 5.
Page 8-38, figure 8-29,
R50: Change reference designator to R51.
R51: Change reference designator to R50.
Schematic 16,
A8U37 pins 10 and 11: Change associated reference designator to U37E.
A8U49: Add value of 6000 ohms to all four associated resistors.
Schematic 17,
A8U14: Change pin 13 to read 12 and change pin 12 to read 13.
A8U18: Change notation A to read C and change notation C to read A.
A8U24: Change notation A to read C and change notation C to read A.
Schematic 18,
A8R28: Change grounded side to be connected to +5V.
Schematic 19,
Signal 78: Show destination schematics of 16, 17, and 18.
Page 8-46, figure 8-34,
R62: Change reference designator to R63.
R63: Change reference designator to R62.
Page 8-46, HORIZONTAL ROM A7U14 TRUTH TABLE,
0: Change to read 1 in 16th line on left-hand side in H0 column,
Schematic 20,
A7U14: Change neumonics of IC as follows:

IC Pin No.	Neumonic
1	G
2	F
3	E
4	D
5	A
6	B
7	C
9	Y4
10	Y3
11	Y2
12	Y1
13	ME1
14	ME2
15	H

Schematic 21,
A7R61: Change value to 680.
A7CR4: Change symbol to resistor. Designate R87, 10 ohms.
A7R62: Change value to 8250.
A7R64: Change value to 47K.
A7R82: Change value to 680.
A7CR3: Change symbol to resistor. Designate R88, 10 ohms.
A7R1: Change value to 8250.
A7R86: Change value to 47K.
A7C11: Change value to 440.
Add: A7R89 (10K) from ground to junction of A7C12/A7U19A.
A7R36: Change value to 10K.
A7R32: Change value to 680.
A7R34: Change value to 8250.
A7R35: Change value to 47K.

OPERATING NOTE CHANGES

MODEL 10231B

SIX BIT DATA PROBE

Operating Note Printed: AUGUST 1974

Make all changes listed below as Errata. Check the following table for your instrument serial prefix and/or serial number and make listed change(s) to the operating note:

Serial Prefix or Number	Make Changes	Serial Prefix or Number	Make Changes

Δ ERRATA

Page 2,
Add: Paragraph 8a as follows:
8a. A pod clip is also supplied with the clock probe. It is intended to be snapped to the coaxial cable behind the circuit pod. The clip can be attached to any secure fixture. The pod clip is used to support the weight of the circuit pod, removing the weight from the hook-type probe assemblies.

Page 3, figure 3,
U1: Pin 2 should read 3, and pin 3 should read 2.
U4: Pin 2 should read 3, and pin 3 should read 2.

Page 4, table 2,
CP1 thru CP6: Change description to PROBE ASSY: Hook Type.
MP6: Change HP Part No. and Mfr Part No. to 1540-0320.
Add: MP7, HP Part No. 5040-0538, HANGER: Circuit Pod, Mfr Code 28480, Mfr Part No. 5040-0538.
W1: Change reference designator to A1W1, and change HP Part No. and Mfr Part No. to 10231-61618.

Page 4, table 2, (Cont'd),
W8: Change to HP Part No. 10231-61619, CABLE: Ground 6 in. with Hook-type Probe Assy, Mfr Code 28480, Mfr Part No. 10231-61619.
Add: W9, HP Part No. 10231-61617, CABLE: Ground 6 in. with alligator clip, Mfr Code 28480, Mfr Part No. 10231-61617.
A1C14 thru A1C19: In description change 0.47 μF to read 0.01 μF.
A1C20: In description change 0.01 μF to read 0.47 μF.
A1E1 thru A1E6: Change description to NUT: Cable Connector With Bead.
A1E7: Change description to NUT: Cable Connector Without Bead.
A1L1 thru A1L6: Delete. These are parts of A1E1 thru A1E6.

12 March 1975
Δ = Latest additions to this change sheet.
This change sheet supersedes all prior change sheets for this operating note.

Supplement A for
10231-90903